Ajay Joshi

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Appointments

Boston University	Department of Electrical and Computer Engineering	Associate Professor, 2016 – present
Google Inc.	Platforms Group	Visiting Research Scientist, 2017 – 2018
Boston University	Department of Electrical and Computer Engineering	Assistant Professor, 2009 – 2016
Boston University	Photonics Center	Member, 2010 – present
Boston University	Hariri Institute for Computing	Member, 2012 – present
Boston University	Center for Computational Neuroscience and Neural Technologies	Steering Committee Member, 2011 – 2016
Massachusetts Institute of Technology	Department of Electrical Engineering and Computer Science	Postdoctoral Associate, 2006 – 2009
Georgia Institute of Technology	Department of Electrical and Computer Engineering	Graduate Research Assistant, 2001 – 2006

Education

Georgia Institute of Technology	Department of Electrical and Computer Engineering	Ph. D., 2006
Georgia Institute of Technology	Department of Electrical and Computer Engineering	M.S., 2003
University of Mumbai, India	Department of Computer Engineering	B. Eng., 2001

Awards and Honors

- NRI Panelist, Vaibhav Summit (organized by Government of India) 2020.
- Google Faculty Research Award 2019, 2018.
- Best Paper Award, ASIA Conference on Computer and Communications Security 2018.
- Boston University Ignition Award 2016.
- IEEE Senior Member.
- Award for Excellence in Teaching, ECE Department, Boston University 2014.
- NSF CAREER Award 2012.
- CELEST / CompNet Prize for Best Poster in Computational Neuroscience at BU Science and Engineering Day 2012.

- Dean's Catalyst Award, College of Engineering, Boston University 2011.
- IEEE Micro Top Pick from Hot Interconnects (for HOTI'08 paper) 2009.
- Best Paper Award Nomination at IEEE/ACM Networks-on-Chip Symposium 2009.
- Recognition Award, Intel Corp, USA 2003.

Research

Current Interests

Computer Architecture, Security, Silicon-Photonic Systems, VLSI Design

Current Projects

- Taming Memory Corruption with Security Monitors (*funded by NSF*)
- Designing multicore 64-bit RISC-V processor (*funded by DARPA*)
- Securing CMOS Integrated Circuits using Nanoantenna-based Optical Watermarks *(funded by Honeywell, NSF and BU OTD)*.
- Reclaiming Dark Silicon using 2.5D Integration (*funded by NSF*)
- MR Spectroscopy for detecting injuries in NFL players and Military subjects (*funded by BWH-BU*)

Past Projects

- Automatically Scalable Computation using Machine Learning *(funded by NSF).*
- System-level Run-time Management Techniques for Energy-efficient Silicon-photonic Manycore Systems *(funded by NSF).*
- Leveraging Intra-chip/Inter-chip Silicon-Photonic Networks for Designing Next-Generation Accelerators *(funded by NSF)*.
- Biologically-inspired hardware for land/aerial robots *(funded by NASA).*
- Design and Evaluation of a Digital Processing Unit for Satellite Angular Velocity Estimation *(funded by MIT Lincoln Scholars Program).*
- Electro-photonic network-on-chip architectures in 1000+ core systems *(funded by DARPA).*
- Application-specific noisy processors: Weaving nearly reliable circuits from an unreliable fabric *(funded by Dean's Catalyst Award).*
- Memristor-based multi-bit memory arrays *(funded partly by NSF CELEST).*
- Next generation solid immersion microscopy for fault Isolation in back-side analysis *(funded by IARPA).*
- Integrated Photonic networks for Manycore systems *(funded by DARPA and Intel).*
- Carbon nanotubes interconnects in VLSI applications *(funded by SRC IFC).*
- Low complexity decoding algorithm for Reed-Solomon code *(funded by NSF).*
- Wave-Pipelined Multiplexed (WPM) Routing for Gigascale Integration (GSI) *(funded by NSF).*

Grants

Current

1. **A. Joshi** and M. Selim Unlu, "Securing CMOS IC Chips using Backside Imaging," *AFRL via Honeywell*, Role: PI, Period: 1/21 – 8/23, Amount - $2,000,000 (Budget approval in progress).
2. **A. Joshi** and V. Reddi, "Designing Custom RISC-V ISA Extensions for Machine Learning Workloads," *Google*, Role: PI, Period: 03/20 – 02/21, Amount - $41,777.
3. M. Egele, **A. Joshi** and W. Robertson, "Taming Memory Corruption with Security Monitors," *NSF*, Role: Co-PI, Period: 07/19 – 6/23, Amount - $1,200,000.
4. M. Taylor, **A. Joshi** and M. Oskin, "WABOSH: Washington and BU do Open Source Hardware," *DARPA*, Role: Co-PI, Contract Period: 6/18 – 5/22, Amount - $2,788,000.

5. A. Coskun, **A. Joshi** and M. Popovic, "Reclaiming Dark Silicon via 2.5D Integrated Systems with Silicon Photonic Networks" *NSF*, Role: Co-PI, Contract Period: 09/17 - 04/21, Amount - $450,000.

Past

6. **A. Joshi** and M. Selim Unlu, "Embedding Optical Nanoantennas in Standard CMOS Cells for Security," *Honeywell*, Role: PI, Period: 7/19 – 11/19, Amount - $48,104.
7. **A. Joshi** and M. Egele, "Securing Processors Using an Array of Specialized and Programmable Policy Engines (ASPEn)," *Google*, Role: PI, Period: 03/19 – 02/20, Amount - $72,457.
8. M. Selim Unlu and **A. Joshi**, "EAGER: Optical Nanoantenna: A Nanotechnology Solution for Advanced Integrated Circuit Testing and Security" *NSF*, Role: Co-PI, Contract Period: 08/16 - 07/18, Amount - $150,209.
9. A. Lin and **A. Joshi**, "Analysis of MR Spectroscopy for the Study of Mild Traumatic Brain Injury in NFL Football Players and Military Subjects" *BU-BWH Biomedical Imaging Training Program,* Role: Co-PI, Contract Period: 06/16 – 05/18, Amount – ~$68,000 (support for 1 graduate student for two years).
10. **A. Joshi**, M. Selim Unlu and Bennett Goldberg, "Detecting Hardware Trojans in Integrated Circuit Chips Using Optical Watermarking" *BU Office of Technology Development*, Role: PI, Contract Period: 5/16 – 4/17, Amount - $50,000.
11. **A. Joshi,** "CNS: CSR Collaborative Research: Leveraging Intra-chip/Inter-chip Silicon-Photonic Networks for Designing Next-Generation Accelerators" *NSF*, Role: PI, Contract Period: 10/15 - 09/18, Amount - $249,828.
12. S. Homer, J. Appavoo and **A. Joshi**, "XPS: FULL: CCA: Collaborative Research: Automatically Scalable Computation," *NSF,* Role: Co-PI, Contract Period: 8/15 - 7/18, Amount - $350,000.
13. **A. Joshi**, "Design and Evaluation of a Digital Processing Unit for Satellite Angular Velocity Estimation" Student Fellowship, *MIT Lincoln Labs*, Role: PI, Contract Period: 9/14 - 12/14, Amount - $18,374.
14. **A. Joshi,** "Biologically-inspired Hardware for Land/Aerial Robots," Student Fellowship, *NASA*, Role: PI, Contract Period: 08/12 - 07/16, Amount - $247,961.
15. **A. Joshi**, "Electro-photonic NEtwork-on-chip Architectures in 1000+ Core systems (ENEAC)" *DARPA through ARMY*, Role: PI, Contract Period: 07/12 - 09/14, Amount - $299,530.
16. **A. Joshi,** "CAREER: System-level Run-time Management Techniques for Energy-efficient Silicon-Photonic Manycore Systems" *NSF CAREER Award*, Role: PI, Contract Period: 04/12 - 03/17, Amount - $469,305.
17. M. Versace and **A. Joshi**, "Neuromorphic Solutions for UAS Collision Avoidance," *NASA,* Role: Co-PI, Contract Period: 03/12 - 03/13, Amount - $59,455.
18. **A. Joshi** and B. Nazer, "Application-Specific Noisy Processors: Weaving Nearly Reliable Circuits from an Unreliable Fabric" *Dean's Catalyst Award, Boston University,* Role: PI, Contract Period: 05/11 - 08/12, Amount- $38,000.
19. M. Versace and **A. Joshi**, "Plastic neuromorphic hardware for autonomous navigation in mobile robots" *NSF CELEST*, Role: Co-I, Contract Period: 04/11 - 03/13, Amount - $224,162.
20. B. Goldberg, S. Unlu, J. Mertz, T. Bifano, R. Ng, T. Kujawa and **A. Joshi**, "Next Generation Solid Immersion Microscopy for Fault Isolation in Back-Side Analysis" *IARPA through AFRL*, Role: Co-I, Contract Period: 11/10 - 11/14, Amount - $4,094,303.
21. **A. Joshi** and A. Coskun, "Power and Performance-Aware Run-Time Management of Manycore Systems" *Intel Corp,* Role: PI*,* Contract Period: 09/10 - 03/12, Intel SCC Equipment.
22. V. Stojanović and **A. Joshi**, "Comparison of Electrical and Optical Interconnects for Energy-efficient Communication in Multi-core Systems," *Intel Corp,* Role: Co-I, Contract Period: 01/08 - 12/10*,* Amount - $450,000.

Publications (My student/postdoc's name is underlined, * indicates co-advised student)
All publications available at www.bu.edu/icsg

Book Chapter

1. Y. Ma, B. Joardar, P. Pande and **A. Joshi**, "Interconnect and Integration Technology" to appear in Emerging Computing: From Devices to Systems - Looking Beyond Moore and Von Neumann, Springer Nature 2021.
2. T. Zhang, J. Klamkin, **A. Joshi** and A. Coskun, "Thermal Management of Silicon Photonic NoCs in Many-core Systems," in Optical Interconnect for Computing Systems, River Publishers 2017.
3. C. Batten, **A. Joshi**, V. Stojanović, and K. Asanović, "Designing Nanophotonic Interconnection Networks," in Integrated Optical Interconnect Architectures and Applications in Embedded Systems, Springer, pp. 81-135, 2013.

Journal

1. B. Zhou, A. Aksoylar, K. Vigil, R. Adato, J. Tan, B. Goldberg, M. Selim Unlu, and **A. Joshi**, "Hardware Trojan Detection using Backside Optical Imaging," to appear in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems.*
2. N. Zaraee, B. Zhou, K. Vigil, M. Shahjamali, **A. Joshi** and M. Selim Unlu, "Gate-level Validation of Integrated Circuits with Structured-Illumination Read-out of Embedded Optical Signatures," *in IEEE Access*, vol. 8, pp. 70900-70912, 2020.
3. D. Petrisko, F. Gilani, M. Wyse, T. Jung, S. Davidson, P. Gao, C. Zhao, Z. Azad, S. Canakci, B. Veluri, T. Guarino, **A. Joshi**, M. Oskin, and M. Taylor, "BlackParrot: An Agile Open Source RISC-V Multicore for Accelerator SoCs," *IEEE Micro* vol. 40, no. 4, pp. 93-102, 2020.
4. A. Coskun, F. Eris, **A. Joshi**, A. B. Kahng, Y. Ma[#], A. Narayan and V. Srinivas, "Cross-Layer Co-Optimization of Network Design and Chiplet Placement in 2.5D Systems," to appear in *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions* **([#]Lead Author)**
5. L. Delshadtehrani*, S. Eldridge, S. Canacki*, M. Egele and **A. Joshi**, "Nile: A Programmable Monitoring Coprocessor," in IEEE Computer Architecture Letters 2018.
6. J. Abellán, A. Coskun, A. Gu, W. Jin, **A. Joshi**, A. Kahng, J. Klamkin, C. Morales, J. Recchio, V. Srinivas and T. Zhang, "Adaptive Tuning of Photonic Devices in a Photonic NoC Through Dynamic Workload Allocation" in *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 36, no.5, pp.801-814, May 2017.
7. A. Ziabari, Y. Sun, Y. Ma, D. Schaa, J. Abellan, R. Ubal, J. Kim, **A. Joshi** and D. Kaeli, "UMH: A Hardware-based Unified Memory Hierarchy for Systems with Multiple Discrete GPUs," *ACM Transactions on Architecture and Code Optimization* vol. 13, no. 4 December 2016.
8. J. Abellán, C. Chen and **A. Joshi**, "Electro-Photonic NoC Designs for Kilocore Systems," to appear in *ACM Journal on Emerging Technologies in Computing Systems (JETC)* vol. 13, no. 2, November 2016.
9. M. Zangeneh and **A. Joshi,** "Designing Tunable Sub-threshold Logic Circuits using Adaptive Feedback Equalization" *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 3, pp. 884-896, March 2016.
10. C. Chen, J. Abellan and **A. Joshi**, "Managing Laser Power in Silicon-Photonic NoC through Cache and NoC Reconfiguration," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol.34, no.6, pp.972-985, June 2015
11. M. Zangeneh and **A. Joshi**, "Design and Optimization of Nonvolatile Multi-bit 1T1R Resistive RAM," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol.22, no.8, pp.1815-1828, Aug. 2014.
12. F. Raudies, S. Eldridge, **A. Joshi** and M. Versace, "Learning to navigate in a virtual world using optic flow and stereo disparity signals," *Artificial Life and Robotics, Springer Japan* Aug. 2014.

13. C. Chen and **A. Joshi**, "Runtime Management of Laser Power in Silicon-Photonic Multibus NoC Architecture," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol.19, no.2, pp.338-350, March-April 2013. **(Invited paper)**
14. Z. Wang*, M. Karpovsky and **A. Joshi**, "Nonlinear Multi-Error Correction Codes for Reliable MLC NAND Flash Memories," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol.20, no.7, pp.1221-1234, July 2012.
15. C. Batten, **A. Joshi**, V. Stojanović, and K. Asanović, "Designing Chip-Level Nanophotonic Interconnection Networks," *Emerging and Selected Topics in Circuits and Systems, IEEE Journal on*, vol.2, no.2, pp.137-153, June 2012.
16. Z. Wang*, M. Karpovsky and **A. Joshi**, "Secure Multipliers Resilient to Strong Fault-Injection Attacks Using Multilinear Arithmetic Codes," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol.20, no.6, pp.1036-1048, June 2012.

Prior to BU

17. C. Batten, **A. Joshi**, J. Orcutt, A. Khilo, B. Moss, C. Holzwarth, M. Popovic, H. Li, H. Smith, J. Hoyt, F. Kartner, R. Ram, V. Stojanović, and K. Asanović, "Building Many-Core Processor-to-DRAM Networks with Monolithic CMOS Silicon Photonics," *Micro, IEEE*, vol.29, no.4, pp.8-21, July-Aug. 2009. **(IEEE Micro Special Issue: Micro's Top Picks from Hot Interconnects 16)**
18. **A. Joshi**, G. Lopez and J. Davis, "Design and Optimization of On-Chip Interconnects Using Wave-Pipelined Multiplexed Routing," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol.15, no.9, pp.990-1002, Sept. 2007.
19. **A. Joshi** and J. Davis, "Wave-pipelined multiplexed (WPM) routing for gigascale integration (GSI)," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol.13, no.8, pp.899-910, Aug. 2005.

Conference/Workshop

1. Y. Ma, L. Delshadtehrani, C. Demirkiran, J. L. Abellan and **A. Joshi**, "TAP-2.5D: A Thermally-Aware Chiplet Placement Methodology for 2.5D Systems," to appear in Proc. *Design, Automation and Test in Europe (DATE)* 2021.
2. L. Delshadtehrani*, S. Canakci*, M. Egele and **A. Joshi**, "SealPK: Sealable Protection Keys for RISC-V," to appear in Proc. *Design, Automation and Test in Europe (DATE)* 2021.
3. T. Baruah, Y. Sun, S. Mojumder, J. Abellan, Y. Ukidave, **A. Joshi**, N. Rubin, J. Kim and D. Kaeli, "Valkyrie: Leveraging Inter-TLB Locality to Enhance GPU Performance," in Proc. *International Conference on Parallel Architectures and Compilation Techniques (PACT)* 2020.
4. A. Narayan, **A. Joshi** and A. Coskun, "Bandwidth Allocation in Silicon Photonic Networks using Application Instrumentation," in Proc. *IEEE High Performance Extreme Computing Conference (HPEC)* 2020.
5. L. Delshadtehrani*, S. Canakci*, B. Zhou, S. Eldridge, **A. Joshi** and M. Egele, "PHMon: A Programmable Hardware Monitor and its Security Applications," in Proc. *USENIX Security Symposium* 2020.
6. S. Canakci*, L. Delshadtehrani*, B. Zhou, **A. Joshi** and M. Egele, "Efficient Context-Sensitive CFI Enforcement through a Hardware Monitor," in Proc. *Conference on Detection of Intrusions and Malware & Vulnerability Assessment (DIMVA)* 2020.
7. M. Louis, E. Coello, H. Liao, **A. Joshi**, and A. Lin, "Quantification of Non-Water-Suppressed Proton Spectroscopy using Deep Neural Networks," in *Proc. International Society for Magnetic Resonance in Medicine (ISMRM)* 2020.

8. A. Narayan, Y. Thonnart, P. Vivet, **A. Joshi** and A. Coskun, "System-level Evaluation of Chip-Scale Silicon-Photonic Networks for Emerging Data-Intensive Applications," in *Proc. Design, Automation and Test in Europe (DATE)* 2020. (Invited paper)
9. T. Baruah, Y. Sun, A. Dincer, S. Mojumder, J. Abellan, Y. Ukidave, **A. Joshi**, N. Rubin, J. Kim and D. Kaeli, "Griffin: Hardware-Software Support for Efficient Page Migration in Multi-GPU systems," in *Proc. International Symposium on High-Performance Computer Architecture (HPCA)* 2020.
10. Z. Azad, M. S. Louis, L. Delshadtehrani, A. Ducimo, S. Gupta, P. Warden, V. J. Reddi and **A. Joshi**, "An End-to-end RISC-V Solution for ML on the Edge Using In-pipeline Support," in *Proc. Boston area ARChitecture (BARC) Workshop* 2020.
11. L. Delshadtehrani*, S. Canakci*, B. Zhou, S. Eldridge, **A. Joshi** and M. Egele, "A Programmable Hardware Monitor for Security of RISC-V Processors" in *Proc. Boston area ARChitecture (BARC) Workshop* 2020.
12. Z. Azad, S. Canakci, S. Davidson, P. Gao, F. Gilani, T. Guarino, T. Jung, D. Petrisko, B. Veluri, M. Wyse, C. Zhao, M. Oskin, M. Bedford Taylor and **A. Joshi**, "BlackParrot: An Open-Source RISC-V Multicore Processor A core for and by the world!" in *Proc. Boston area ARChitecture (BARC) Workshop* 2020.
13. Y.Sun, T. Baruah, S. Mojumder, S. Dong, X. Gong, S. Treadway, Y. Bao, S. Hance, C McCardwell, V. Zhao, H. Barclay, A. Ziabari, Z. Chen, R. Ubal, J. Abellán, J. Kim, **A. Joshi**, D. Kaeli, "MGPUSim: Enabling Multi-GPU Performance Modeling and Optimization," in *Proc. International Symposium on Computer Architecture (ISCA)* 2019.
14. M. Louis, Z. Azad, L. Delshadtehrani, P. Warden, V. Reddi, S. Gupta and **A. Joshi**, "Towards Deep Learning using TensorFlow Lite on RISC-V," in *Proc. Workshop on Computer Architecture Research with RISC-V (CARRV)* held in conjunction with *International Symposium on Computer Architecture (ISCA)* 2019.
15. Z. Azad, L. Delshadtehrani, F. Gilani, T. Jung, K. Lim, D. Petrisko, M. Wyse[#], B. Zhou, T. Guarino, B. Veluri, Y. Wang, M. Oskin, **A. Joshi**, M. Taylor, "The BlackParrot Processor: An Open-Source Industrial-Strength RV64G Multicore Processor," in *Government Microcircuit Application's Critical Technology Conference (GOMACTech)* 2019. **([#]Lead Author)**
16. S. Mojumder, M. Louis, Y. Sun, A. Ziabari, J. Abellan, J. Kim, D. Kaeli and **A. Joshi**, "Evaluation of Volta-based DGX-1 System Using DNN Workloads," in *Proc. Boston area ARChitecture (BARC) Workshop* 2019.
17. B. Zhou, A. Gupta[*], R. Jahanshahi, M. Egele and **A. Joshi**, "Can We Reliably Detect Malware Using Hardware Performance Counters?," in *Proc. Boston area ARChitecture (BARC) Workshop* 2019.
18. A. Coskun, F. Eris[#], **A. Joshi**, A. Kahng, Y. Ma and V. Srinivas, "A Cross-Layer Methodology for Design and Optimization of Networks in 2.5D Systems," *in Proc. International Conference on Computer-Aided Design (ICCAD)* 2018. **([#]Lead Author)**
19. S. Mojumder, M. Louis, Y. Sun, A. Ziabari, J. Abellan, J. Kim, D. Kaeli and **A. Joshi**, "Profiling DNN Workloads on a Volta-based DGX-1 System," *in Proc. IEEE International Symposium on Workload Characterization (IISWC)* 2018.
20. B. Zhou, A. Gupta[*], R. Jahanshahi, M. Egele and **A. Joshi**, "Hardware Performance Counters Can Detect Malware: Myth or Fact?," in *Proc. ACM Asia Conference on Computer and Communications Security (ASIACCS)* 2018. **(Best Paper Award)**
21. M. Louis, M. Alosco, B. Rowland, H. Liao, J. Wang, R. Stern, **A. Joshi**, and A. Lin, "Biomarkers for CTE diagnosis in retired NFL players using Machine learning" in *Proc. International Society for Magnetic Resonance in Medicine,* 2018. **(Summa Cum Laude Merit Award)**

22. F. Eris, **A. Joshi**, A. Kahng, Y. Ma[#], S. Mojumder and T. Zhang, "Leveraging Thermally-Aware Chiplet Organization in 2.5D Systems to Reclaim Dark Silicon," in *Proc. Design, Automation and Test in Europe (DATE)* 2018. **([#]Lead Author)**
23. A. Coskun, F. Eris, **A. Joshi**, A. Kahng, Y. Ma, S. Mojumder and T. Zhang, "Reclaiming Dark Silicon Using Thermally-Aware Chiplet Organization in 2.5D Integrated Systems," in Proc. *Boston area ARChitecture (BARC) Workshop* 2018.
24. M. Louis, M. Alosco, B. Rowland, H. Liao, J. Wang, I. Koerte, M. Shenton, R. Stern, **A. Joshi** and A. Lin, "Using Machine Learning Techniques for Identification of Chronic Traumatic Encephalopathy Related Spectroscopic Biomarkers," in *Applied Imagery Pattern Recognition Workshop on Big Data, Analytics and Beyond* 2017.
25. B. Zhou, M. Egele and **A. Joshi**, "High-Performance Low-Energy Implementation of Cryptographic Algorithms on a Programmable SoC for IoT Devices," in *IEEE High Performance Extreme Computing Conference (HPEC)* 2017.
26. L. Delshadtehrani, J. Appavoo, M. Egele, **A. Joshi** and S. Eldridge, "Varanus: An Infrastructure for Programmable Hardware Monitoring Units," *Proc. Boston area ARChitecture (BARC) Workshop* 2017.
27. Z. Takhirov, J. Wang, V. Saligrama and **A. Joshi**, "Energy-Efficient Classification: Adaptive Approach," *Proc. Boston area ARChitecture (BARC) Workshop* 2017.
28. Z. Takhirov, J. Wang, V. Saligrama and **A. Joshi**, "Energy-Efficient Adaptive Classifier Design for Mobile Systems," *Proc. International Symposium on Low Power Electronics and Design (ISLPED)* 2016.
29. A. Coskun, A. Gu, W. Jin, **A. Joshi**, A. B. Kahng, J. Klamkin, Y. Ma, J. Recchio, V. Srinivas and T. Zhang, "Cross-Layer Floorplan Optimization For Silicon Photonic NoCs In Many-Core Systems", *Proc. Design, Automation and Test in Europe (DATE)* 2016.
30. S. Eldridge, T. Unger, M. Louis, A. Waterland, M. Seltzer, J. Appavoo and **A. Joshi**, "Neural Networks as Function Primitives: Software/Hardware Support with X-FILES/DANA," *Proc. Boston area ARChitecture (BARC) Workshop* 2016.
31. S. Eldridge, A. Waterland, M. Seltzer, J. Appavoo and **A. Joshi**, "Towards General-Purpose Neural Network Computing," *Proc. Parallel Architectures and Compilation Techniques (PACT)* 2015.
32. R. Adato, A. Uyar, M. Zangeneh, B. Zhou, **A. Joshi,** B. Goldberg and M. Selim Unlu, "Integrated Nanoantenna Labels for Rapid Security Testing of Semiconductor Circuits," Proc. *Frontiers in Optics* 2015.
33. A. Ziabari, J. Abellán, Y. Ma, **A. Joshi** and D. Kaeli, "Asymmetric NoC Architectures for GPU Systems," *Proc. International Symposium on Networks-on-Chip (NOCS)* 2015.
34. B. Zhou, R. Adato, M. Zangeneh, T. Yang, A. Uyar, B. Goldberg, M. S. Unlu, **A. Joshi,** "Detecting Hardware Trojans Using Backside Optical Imaging of Embedded Watermarks," *Proc. Design Automation Conference (DAC)* 2015.
35. A. Ziabari, J. Abellan, R. Ubal, C. Chen, **A. Joshi** and D. Kaeli, "Leveraging Silicon-Photonic NoC for Designing Scalable GPUs," *Proc. International Conference on Supercomputing (ICS)* 2015.
36. T. Cilingiroglu, M. Zangeneh, A. Uyar, W. Clem Karl, J. Konrad, **A. Joshi**, B. Goldberg and M. Selim Unlu, "Dictionary-based Sparse Representation for Resolution Improvement in Laser Voltage Imaging of CMOS Integrated Circuits," in *Proc. Design, Automation and Test in Europe (DATE)* 2015.
37. S. Eldridge and A. Joshi, "Exploiting Hidden Layer Modular Redundancy for Fault-Tolerance in Neural Network Accelerators," *Proc. Boston area ARChitecture (BARC) Workshop* 2015.
38. C. Chen, T. Zhang, P. Contu, J. Klamkin, A. Coskun, and **A. Joshi**, "Sharing and Placement of On-chip Laser Sources in Silicon-Photonic NoCs," *Networks-on-Chip (NoCS), 2014 Eighth IEEE/ACM International Symposium on*, vol., no., pp.88-95, 17-19 Sept. 2014.

39. J. Appavoo, A. Waterland, S. Eldridge, K. Zhao, **A. Joshi**, S. Homer and M. Seltzer, "Programmable Smart Machines: A Hybrid Neuromorphic approach to General Purpose Computation" *Neuromorphic Architectures (NeuroArch) Workshop at 41th International Symposium on Computer Architecture (ISCA-41)* 2014.
40. S. Eldridge, F. Raudies, D. Zou and **A. Joshi**, "Neural Network-Based Accelerators for Transcendental Function Approximation," In *Proceedings of the 24th edition of the Great Lakes Symposium on VLSI (GLSVLSI 2014).* ACM, New York, NY, USA, 169-174.
41. M. Zangeneh and **A. Joshi**, "Sub-threshold Logic Circuit Design using Feedback Equalization," *Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014* , vol., no., pp.1,6, 24-28 March 2014.
42. T. Zhang, J. Abellan, **A. Joshi** and A. Coskun, "Thermal Management of Manycore Systems with Silicon-Photonic Networks," *Design, Automation and Test in Europe Conference and Exhibition (DATE), 2014* , vol., no., pp.1,6, 24-28 March 2014.
43. C. Chen, **A. Joshi** and E. Salminen, "Profiling EEMBC MultiBench Programs using Full-system Simulations," *Proc. Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW-5) at 20th International Symposium On High Performance Computer Architecture (HPCA-20)* 2014.
44. Z. Takhirov, B. Nazer and **A. Joshi**, "Energy-Efficient Pass-Transistor-Logic Using Decision Feedback Equalization," *Low Power Electronics and Design (ISLPED), 2013 IEEE International Symposium on* , vol., no., pp.335,340, 4-6 Sept. 2013.
45. S. Eldridge, F. Raudies and **A. Joshi**, "Approximate Computation using Neuralized FPU," *Brain-Inspired Computing (BIC) Workshop at 40th International Symposium on Computer Architecture (ISCA-40)* 2013.
46. **A. Joshi**, C. Chen, Z. Takhirov and B. Nazer, "A Multi-layer Approach to Green Computing: Designing Energy-efficient Digital Circuits and Manycore Architectures," *Proc. Workshop on Lighter-than-Green Dependable Multicore Architectures (LGDMA), Held in conjunction with International Green Computing Conference (IGCC)* 2012. **(Invited paper)**
47. M. Motter, M. Versace, and **A. Joshi**, "Neuromorphic solutions for UAS collision avoidance," *Proc. International Conference on Cognitive and Neural Systems (ICCNS)* 2012.
48. M. Zangeneh and **A. Joshi**, "Performance and Energy Models for Memristor-based1T1R RRAM Cell," In *Proceedings of the Great Lakes Symposium on VLSI (GLSVLSI 2012).* ACM, New York, NY, USA, 9-14.
49. Z. Takhirov, B. Nazer and **A. Joshi**, "Error Mitigation in Digital Logic using Feedback Equalization with Schmitt Trigger (FEST) Circuit," *Quality Electronic Design (ISQED), 2012 13th International Symposium on*, vol., no., pp.312,319, 19-21 March 2012.
50. Z. Takhirov, B. Nazer and **A. Joshi**, "A Preliminary Look at Error Avoidance in Digital Logic Via Feedback Equalization," in *Proc. Allerton-11* 2011. **(Invited paper)**
51. C. Chen, J. Meng, A. Coskun and **A. Joshi**, "Express Virtual Channels with Taps (EVC-T): A Flow Control Technique for Network-on-Chip (NoC) in Manycore Systems," *High Performance Interconnects (HOTI), 2011 IEEE 19th Annual Symposium on* , vol., no., pp.1,10, 24-26 Aug. 2011.
52. Z. Wang*, M. Karpovsky and **A. Joshi**, "Influence of Metallic Tubes on the Reliability of CNTFET SRAMs: Error Mechanisms and Countermeasures," In *Proceedings of the 21st edition of the Great Lakes Symposium on VLSI (GLSVLSI 2011).* ACM, New York, NY, USA, 359-362.
53. J. Meng, C. Chen, A. Coskun and **A. Joshi**, "Run-Time Energy Management of Manycore Systems Through Reconfigurable Interconnects," In *Proceedings of the 21st edition of the Great Lakes Symposium on VLSI (GLSVLSI 2011).* ACM, New York, NY, USA, 43-48.
54. S. Beamer, C. Sun, Y. Kwon, **A. Joshi**, C. Batten, V. Stojanović, K. Asanović, "Re- Architecting a DRAM Memory Channel with Monolithically Integrated Silicon Photonics," In *Proceedings of the*

37th annual international symposium on Computer architecture (*ISCA-37*) 2010. ACM, New York, NY, USA, 129-140.

55. Z. Wang*, M. Karpovsky, **A. Joshi**, "Reliable MLC NAND Flash Memories Based on nonlinear t-Error-Correcting Codes," *Dependable Systems and Networks (DSN), 2010 IEEE/IFIP International Conference on*, vol., no., pp.41,50, June 28 2010-July 1 2010.
56. V. Stojanović, **A. Joshi**, C. Batten, Y.-J. Kwon, S. Beamer, S. Chen, and K. Asanović, "Design-space exploration for CMOS photonic processor networks," *Optical Fiber Communication (OFC), collocated National Fiber Optic Engineers Conference, 2010 Conference on (OFC/NFOEC)*, vol., no., pp.1-3, 21-25 March 2010.
57. V. Stojanović, **A. Joshi**, C. Batten, Y.-J. Kwon, S. Beamer, S. Chen and K. Asanović, "CMOS photonic processor-memory networks," *Photonics Society Winter Topicals Meeting Series (WTM), 2010 IEEE*, vol., no., pp.118-119, 11-13 Jan. 2010.
58. Z. Wang*, M. Karpovsky, B. Sunar, and **A. Joshi**, "Design of Reliable and Secure Multipliers by Multilinear Arithmetic Codes," *Proc. Int. Conf. on Information, Communications and Signal Processing (ICICSP),* pp. 47-62 Dec. 2009.
59. **A. Joshi**, C. Batten, Y. Kwon, S. Beamer, I. Shamim, K. Asanović and V. Stojanović, "Limits and Opportunities for Designing Manycore Processor-to-Memory Networks using Monolithic Silicon Photonics" *Workshop on Photonic Interconnects & Computer Architecture. Held in Conjunction with 42nd Annual ACM/IEEE International Symposium on Microarchitecture, (MICRO-42)* 2009.
60. **A. Joshi**, C. Batten, Y.-J. Kwon, S. Beamer, I. Shamim, K. Asanović and V. Stojanović, "Designing Manycore Processor Networks using Silicon Photonics," *LEOS Annual Meeting Conference Proceedings, 2009. (LEOS '09) IEEE*, vol., no., pp.16-17, 4-8 Oct. 2009.

Prior to BU

61. **A. Joshi**, B. Kim and V. Stojanović, "Designing Energy-efficient Low-Diameter On-chip Networks with Equalized Interconnects," *High Performance Interconnects, 2009. (HOTI 2009) 17th IEEE Symposium on* , vol., no., pp.3,12, 25-27 Aug. 2009.
62. S. Beamer, K. Asanović, C. Batten, **A. Joshi**, and V. Stojanović, "Designing Multi-socket Systems Using Silicon Photonics," In *Proceedings of the 23rd international conference on Supercomputing (ICS 2009)* ACM, New York, NY, USA, 521-522.
63. V. Stojanović, **A. Joshi**, C. Batten, J. Kwon and K. Asanović, "Manycore Processor Networks with Monolithic Integrated CMOS Photonics," *in Conference on Lasers and Electro-Optics/International Quantum Electronics Conference, OSA Technical Digest (CD) (Optical Society of America, 2009),* paper CTuC3. **(Invited paper)**
64. **A. Joshi**, F. Chen and V. Stojanović, "A Modeling and Exploration Framework for Interconnect Network Design in the Nanometer Era," *Networks-on-Chip, 2009. (NoCS 2009) 3rd ACM/IEEE International Symposium on* , vol., no., pp.91,91, 10-13 May 2009.
65. **A. Joshi**, C. Batten, Y. Kwon, S. Beamer, I. Shamim, K. Asanović and V. Stojanović, "Silicon-Photonic Clos Networks for Global On-Chip Communication," *Networks-on-Chip, 2009 (NoCS 2009) 3rd ACM/IEEE International Symposium on*, vol., no., pp.124,133, 10-13 May 2009 **(Nominated for Best Paper Award)**.
66. C. Batten, **A. Joshi**, J. Orcutt, A. Khilo, B. Moss, C. Holzwarth, M. Popovic, H. Li, H. Smith, J. Hoyt, F. Kaertner, R. Ram, V. Stojanović, and K. Asanović, "Building Manycore Processor-to-DRAM Networks with Monolithic Silicon Photonics," *High Performance Interconnects, 2008. (HOTI 2008) 16th IEEE Symposium on* , vol., no., pp.21,30, 26-28 Aug. 2008.
67. F. Chen, **A. Joshi**, V. Stojanović and A. Chandrakasan, "Scaling and Evaluation of Carbon Nanotube Interconnects for VLSI Applications," In *Proceedings of the 2nd international conference on Nano-Networks* (*Nano-Net 2007*).

68. D. Sekar, R. Venkatesan, K. Bowman, **A. Joshi**, J. Davis and J. Meindl, "Optimal repeaters for sub-50nm interconnect networks," *Interconnect Technology Conference, International (IITC 2006)*, vol., no., pp.199,201, 5-7 June 2006.
69. **A. Joshi**, V. Deodhar and J. Davis, "Low Power Multilevel Interconnect Networks Using Wave-Pipelined Multiplexed (WPM) Routing," *VLSI Design, 2006. Held jointly with 5th International Conference on Embedded Systems and Design., 19th International Conference on* , vol., no., pp.4 pp.,, 3-7 Jan. 2006.
70. J. Davis, V. Deodhar and **A. Joshi**, "The Impact of Wave Pipelining on Future Interconnect Technologies," *Proc. Advanced Metallization Conference* 2005 **(Invited paper)**.
71. **A. Joshi** and J. Davis, "Gigascale ASIC/SoC Design using Wave-Pipelined Multiplexed (WPM) Routing," *SOC Conference, 2005. Proceedings. IEEE International*, vol., no., pp.137,142, 19-23 Sept. 2005
72. **A. Joshi** and J. Davis, "Wave-Pipelined 2-Slot Time Division Multiplexed (WP/2-TDM) Routing," In *Proceedings of the 15th ACM Great Lakes Symposium on VLSI* (*GLSVLSI 2005*). ACM, New York, NY, USA, 446-451.
73. **A. Joshi** and J. Davis, "A 2-Slot Time-Division Multiplexing (TDM) Interconnect Network for Gigascale Integration (GSI)," In *Proceedings of the 2004 international workshop on System level Interconnect Prediction* (*SLIP 2004*). ACM, New York, NY, USA, 64-68.

Technical Reports/ArXiv Uploads

1. S. A. Mojumder, Y. Sun, L. Delshadtehrani, Y. Ma, T. Baruah, J. L. Abellán, J. Kim, D. Kaeli and **A. Joshi**, "MGPU-TSM: A Multi-GPU System with Truly Shared Memory," arXiv preprint arXiv:2008.02300, 2020.
2. F. Eris, S. Canakci, C. Demirkiran and **A. Joshi**, "Custom Tailored Suite of Random Forests for Prefetcher Adaptation," arXiv preprint arXiv:2008.00176, 2020.
3. S. A. Mojumder, Y. Sun, L. Delshadtehrani, Y. Ma, T. Baruah, J. L. Abellán, J. Kim, D. Kaeli and **A. Joshi**, "HALCONE: A Hardware-Level Timestamp-based Cache Coherence Scheme for Multi-GPU system," arXiv preprint arXiv:2007.04292, 2020.
4. Y. Sun, T. Baruah, S. A. Mojumder, S. Dong, R. Ubal, X. Gong, S. Treadway, Y. Bao, V. Zhao, J. L. Abellan, J. Kim, **A. Joshi** and D. Kaeli, "Mgsim+ mgmark: A framework for multi-gpu system research," arXiv preprint arXiv:1811.02884, 2018.
5. Z. Takhirov, J. Wang, M. Louis, V. Saligrama and **A. Joshi** "Field of Groves: An Energy-Efficient Random Forest," arXiv preprint arXiv:1704.02978, 2017.
6. R. Adato, A. Uyar, M. Zangeneh, B. Zhou, **A. Joshi**, B. Goldberg and M. S. Unlu, "Rapid mapping of digital integrated circuit logic gates via multi-spectral backside imaging," arXiv preprint arXiv:1605.09306, 2016.
7. F. Raudies, S. Eldridge, **A. Joshi** and M. Versace, "Reinforcement Learning of Visual Navigation Using Distances Extracted from Stereo Disparity or Optic Flow" (Boston University ECE-2013-1)
8. S. Beamer, C. Sun, Y. Kwon, **A. Joshi**, C. Batten, V. Stojanović and K. Asanović, "Re-architecting DRAM with Monolithically Integrated Silicon Photonics" (UC Berkeley EECS-2009-179)

Tutorials

1. **A. Joshi**, "Designing Silicon-Photonic Communication Networks for Manycore Systems," VLSI Design 2012.
2. **A. Joshi**, R. Ho and M. Farrens, "Silicon Photonics Circuits and Architectures for ManyCore Systems" VLSI-SoC 2012.

Patents

1. R. Ramaraju**, A. Joshi** and B. Nazer, "Hierarchical Error Correction," 2014.
2. R. Adato, **A. Joshi**, M. S. Unlu, B. Goldberg, "Gate-level mapping of integrated circuits using multi-spectral imaging," 2018.

Invited Talks/Presentations (Paper presentations at conferences/workshops not included)

1. "Electrical and Photonic Networks for 2.5D Integrated Systems," International Symposium on Microelectronics, October 2020.
2. "Programmable Hardware Monitors for Software Security," IIT Mumbai, India, August 2019.
3. "Silicon Photonic Networks for GPUs," North American Workshop on Silicon Photonics for High Performance Computing, May 2019.
4. "Do you plan to use Machine Learning? Proceed with caution!", NOPE Workshop, Co-located with ASPLOS 2019, April 2019.
5. "Programmable Hardware Monitors for Software Security," Draper, February 2019.
6. "BlackParrot: An Open Source RISC-V Multicore Processor for and by the World," Red Hat Collaboratory at Boston University Microarchitecture Workshop, February 2019.
7. "Programmable Hardware Monitors for Software Security," Texas A&M University, January 2019.
8. "Electro-Photonic Networks for Kilocore Systems," Emerging Technologies Conference, May 2018.
9. "Designing Energy-efficient and Secure Accelerators for Machine Learning Applications," University of Southern California, October 2016.
10. "Energy-efficient Computing at the Edge of the Internet-of-Things (IoT)," Indian Institute of Science, India, August 2016.
11. "Can Silicon Photonics Illuminate the Dark Silicon Age?" Invited talk at Energy-efficient Computing in the Dark Silicon Era Workshop, co-located with IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 2015.
12. "Computing in the Energy-constrained Era: From Ultra-low Power Equalized Logic Circuits to Energy-efficient Silicon-Photonic NoC Architectures," University of Colorado, Boulder, October 2015.
13. "Run-time Strategies for Energy-efficient Operation of Silicon-Photonic NoC," Invited talk at the Symposium on High-Performance Interconnects, August 2015.
14. "Pushing the energy-efficiency envelope: Designing ultra-low power equalized logic circuits and energy-efficient silicon-photonic NoC architectures," École Polytechnique Fédérale de Lausanne (EPFL), March 2015.
15. "Run-time and Design-time Strategies for Energy-efficient Operation in Silicon-Photonic NoCs," DRDO (India), December 2014.
16. "Run-time and Design-time Strategies for Energy-efficient Operation in Silicon-Photonic NoCs," Columbia University, November 2014.
17. "ABHA: Manycore Processor with Optical Network-on-Chip," DRDO (India), February 2014.
18. "Designing Energy-efficient Manycore Systems Using Equalized Logic Circuits and Silicon-Photonic NoC Architectures," Intel Corporation, May 2013.
19. "Designing Energy-efficient Silicon-photonic NoC for Manycore Systems," Worcester Polytechnic Institute, September 2012.
20. "A Multi-layer Approach to Green Computing: Designing Energy-efficient Digital Circuits and Manycore Architectures," Invited talk at the Workshop on Lighter-than-Green Dependable Multicore Architectures (LGDMA), June 2012.
21. "Brain-inspired Computing using Nanoscale Memristors" NANOvember, Boston University, November 2011.

22. "A Modeling and Exploration Framework for Interconnect Network Design with CNT, graphene and copper channels," IFC-FCRP Workshop on: On-Chip Connectivity for End-of-Roadmap CMOS, CNSE, University of Albany, June 2009.
23. "Silicon-Photonic Clos Networks for Global On-Chip Communication," CIPS workshop, Massachusetts Institute of Technology, May 2009.
24. "Interconnect Design: From Emerging Devices to Energy-efficient Networks," Boston University, February 2009.
25. "Interconnect Design: From Emerging Devices to Energy-efficient Networks," Northeastern University, February 2009.
26. "Building manycore processor-to-DRAM networks using monolithic silicon photonics," Boston University, October 2008.
27. "Interconnect design in modern VLSI systems," India Institute of Technology, Mumbai, August 2008.
28. "Interconnect design in modern VLSI systems," Drexel University, March 2008.
29. "Wave-Pipelined Multiplexed (WPM) routing for Gigascale Integration (GSI)," University of Washington, June 2006.

Media coverage

1. C. Humphries, "Brainy, but so artificial," BU Research Magazine, Fall 2011.
2. T. Simonite, "Computing at the speed of light," MIT Technology Review, posted Aug 4, 2010.
3. R. Wilson (Executive Editor), "Heard at Hot Interconnects: Multicore SoCs may require optical interconnect," EDN News, posted Aug 27, 2008.

Professional Activities

1. Associate Editor for IEEE Transactions on VLSI Systems 2019 - present.
2. General Chair for Networks-on-Chip Symposium 2020.
3. Technical Program Committee Chair for Networks-on-Chip Symposium 2019.
4. Workshop Organizer - Boston Area ARChitecture Workshop 2015 (http://www.bu.edu/barc2015).
5. NSF review panels 2011, 2012, 2013, 2016, 2017, 2020.
6. Proposal reviewer for Army Research Office 2014.
7. Proposal reviewer for ETH Zurich Research Commission 2013.
8. Associate Editor
    a. Journal of Circuits, Systems and Computers 2012, 2013.
9. Special Sessions Chair for Great Lakes Symposium on VLSI 2016.
10. Design Contest Chair
    a. International Symposium on Low Power Electronic Design 2020
11. Technical Program Committee Member
    a. Design Automation Conference 2017, 2018, 2019
    b. Design, Automation and Test in Europe 2017, 2018, 2019, 2020, 2021
    c. International Conference on Computer Aided Design 2019, 2020
    d. International Conference on Computer Design 2020
    e. International Symposium on Low Power Electronic Design 2020
    f. Symposium on High-Performance Interconnects 2010, 2011, 2013, 2014, 2015, 2016, 2017
    g. International Symposium on Networks-on-Chip 2014, 2015, 2016, 2017, 2018
    h. International Symposium on Quality Electronic Design 2013, 2014, 2015, 2016.
    i. International Green Computing Conference 2014, 2015.
    j. International Conference on VLSI Design 2011, 2012, 2013, 2014, 2015.
    k. Workshop on the Interaction between Nanophotonic Devices and Systems 2010.

12. Reviewer
    a. MICRO 2020, HPCA 2019, HPCA 2018, MICRO 2017, ISCA 2017, HPCA 2017, MICRO 2016, HPCA 2016, ISCA 2015, HPCA 2014, DAC 2014, DAC 2013, DAC 2012, ISCAS 2011, MWSCAS 2008
    b. IEEE Trans. VLSI Systems.
    c. IEEE Trans Circuits and Systems.
    d. IEEE Journal of Solid-State Circuits.
    e. IEEE Transactions on CAD.
    f. IEEE Computer Architecture Letters.
    g. IEEE Transactions on Computer.
    h. IEEE Transactions on Parallel and Distributed Systems
    i. IEEE Photonics Technology Letters.
    j. Journal of Parallel and Distributed Computing.
    k. IEEE Journal for Emerging and Selected Topics in Circuits and Systems.
    l. IEEE Journal of Selected Topics in Quantum Electronics.
    m. ACM Transactions on Architecture and Code Optimization.
    n. IEEE D&T Special Issue on Silicon Nanophotonics for Future Multicore Architectures.
    o. IET Circuits, Devices & Systems 2008
13. Session Chair
    a. (TuB) for IEEE/Photonics Society Meeting 2009
    b. International Conference on VLSI Design 2012
    c. International Symposium on Networks-on-Chip 2013
    d. International Symposium on Networks-on-Chip 2015
    e. Design Automation Conference 2018
14. Publicity Chair
    a. MICRO Symposium 2013
15. Member of the OCP-IP NoC Benchmarking Workgroup (2010-2011)
16. Member of the Postdoctoral advisory council, MIT (2007-2008)
17. Member of IEEE since 1998

PhD Research advisees (Current and Past)

Current:

Saiful Mojumder (Expected Graduation Semester: Fall 2020)
Leila Delshadtehrani (co-advised with Manuel Egele) (Expected Graduation Semester: Spring 2021)
Marcia Sahaya Louis (co-advised with Alexander Lin) (Expected Graduation Semester: Spring 2020)
Furkan Eris (Expected Graduation Semester: Spring 2021)
Sadullah Canacki (co-advised with Manuel Egele) (Expected Graduation Semester: Spring 2021)
Zahra Azad (Expected Graduation Semester: Spring 2022)
Cansu Demirkiran (Expected Graduation Semester: Spring 2024)
Rashmi Agrawal (Expected Graduation Semester: Spring 2022)
Chathura Niroshan (Expected Graduation Semester: Spring 2025)

Past:

Yenai Ma, PhD 2020 → Google
Boyou Zhou, PhD 2019 → Analog Garage → Amazon
Zafar Takhirov, PhD 2017 → Didi Research → Facebook
Schuyler Eldridge, PhD 2016 → Postdoc at IBM T J Watson → SiFive

Mahmoud Zangeneh, PhD 2015 → Postdoc at UC Santa Barbara → Shore Western → Ancra → FormFactor
Chao Chen, PhD 2014 → Freescale Semiconductor → Qualcomm
Zhen Wang, PhD 2011 (co-advised with Mark Karpovsky) → Mediatek → The Mathworks Inc.

Postdoc advisees
Past:
Jose L. Abellan Postdoc 2012-2014 → Asst. Professor at Catholic University of Murcia (Spain)

MS/MEng Research advisees (Current and Past)
Current:
NA

Past:
John Burke, MS 2017 → Draper Labs
Anmol Gupta, MS 2017 → Analog Devices Inc.
Luke Osborne MS 2017 → MITRE
Tony Ye, MS 2016 (TBD)
Kanchan Gupta, MS 2015 → PhD Student at NYU
Jeffrey Little, MS 2014 → MIT Lincoln Labs
Florian Raudies, MS 2014 → HP Labs
Guoqi Lu, MS 2014 → Juniper Networks
Michael Kasparian, MS 2013 → Atlas Wearables
Anusha Madala, MS 2011 → Intel
Chaitanya BSK, MS 2011 → Netronome Systems

BS Research advisees (Current and Past)
Current:
Devin Bidstrup
Vineet Kotariya (IIT Bombay)

Past:
Alex Hammerman → US Army
Ryan Hoffman
DJ Morel
Sami Shahin → Graduate School at BU
Timothy Chong → PhD student at Stanford
Jian Tan → US Navy
Zhanna Kaufmann, BS 2015 → MITRE
David Zou, BS 2014 → Intrepid Pursuits
Kate Thurmer, LEAP 2013 → MIT Lincoln Labs

BU RISE advisees (Past)
Raj Palleti, BU RISE Intern 2019 (Stanford undergraduate student starting Fall 2020)
Katie Bacher, BU RISE Intern 2015 (MIT undergraduate student starting Fall 2016)
Gary Li, BU RISE Intern 2015 (U C Berkeley undergraduate student starting Fall 2016)
Adit Deshpande, BU RISE Intern 2014 (UCLA undergraduate student starting Fall 2015)
Tanmay Ghai, BU RISE Intern 2014 (U C Berkeley undergraduate student starting Fall 2015)

Aamir Rasheed, BU RISE Intern 2013 (now a UCSD undergraduate student)
Kevin Chen, BU RISE Intern 2012 (now a USC undergraduate student)
Eleanor Pence, BU RISE Intern 2012
Vincent Kee, BU RISE Intern 2011 (now a MIT undergraduate student)
Samuel Kim, BU RISE Intern 2011 (now a UC Berkeley undergraduate student)

Awards/Fellowships/Honors to my students

- Leila Delshadtehrani: Invited to present her work on programmable hardware monitors at the FOCA workshop organized by IBM Research.
- Leila Delshadtehrani: Awarded the GHC Student Scholarship to attend the 2020 Virtual Grace Hopper Celebration.
- Devin Bidstrup: Undergraduate Research Opportunities Program's Student Research Award, Summer 2020, Fall 2020.
- Leila Delshadtehrani: Best Paper Award (3rd place) at the CISE Graduate Student Workshop (CGSW) 2020.
- Ryan Hoffman: Undergraduate Research Opportunities Program's Student Research Award, Fall 2019.
- D J Morel: Undergraduate Research Opportunities Program's Student Research Award, Summer 2019.
- Alexander Hammerman: Undergraduate Research Opportunities Program's Student Research Award, Fall 2018 and Spring 2019.
- Marcia Sahaya Louis: ISMRM Summa Cum Laude Merit Award 2018.
- Alexander Hammerman: Boston University College of Engineering's Lutchen Fellowship, Summer 2018.
- Marcia Sahaya Louis: Research Excellence Award, Discover Brigham 2017, November 2017.
- Sami Shahin: Undergraduate Research Opportunities Program's Student Research Award, Summer 2016.
- Mahmoud Zanganeh: Boston University Department of ECE's Outstanding Ph.D. Dissertation Award 2015.
- Timothy Chong: Boston University College of Engineering's Lutchen Fellowship, Summer 2015.
- Zhanna Kaufman: Undergraduate Research Opportunities Program's Student Research Award, Fall 2014 and Spring 2015.
- Timothy Chong: Undergraduate Research Opportunities Program's Student Research Award, Fall 2013.
- David Zou: Boston University College of Engineering's Lutchen Fellowship, Summer 2013.
- Kate Thurmer: Undergraduate Research Opportunities Program's Student Research Award, Fall 2012.
- Schuyler Eldridge: NASA Space Technology Research Fellowship 2012 (renewable up to 3 years).

Teaching

Boston University - Boston, MA

- EK131/132 (Introduction to Engineering - Electronic Control of Robots) - *Fall 2011, Fall 2012, Spring 2014, Spring 2015, Spring 2016*.
  The goal of this course is to expose students to electrical devices, circuit design, digital logic design and programming of embedded computer systems. Using robotics as an underlying theme, students get hands-on experience working on lab assignments designed around each of these areas of Electrical and Computer Engineering. By the end of the semester, students get first-hand experience

in designing and programming a robot to solve a class application challenge. **I designed this new section for EK131/132 in Fall 2011.**

- EC311 (Introduction to Logic Design) - *Fall 2010, Spring 2012, Fall 2018, Fall 2019*
  The class covers the theory and practice of digital hardware design. Students learn to formulate real world tasks using Boolean algebra and FSM theory, and to apply manual and computer-aided techniques to solve the problems. In addition, they also learn fundamental circuit design and verification skills using Verilog HDL and FPGAs.

- EC513 (Computer Architecture) – *Spring 2017, Spring 2020, Fall 2020*
  The goal of this course is to learn the design of modern computer system architecture and develop a strong platform that could be leveraged to design future computer systems. The course covers pipelined processors, ISAs (instruction set architectures), evaluation metrics and trends, performance and cost issues, memory hierarchies (caches, virtual memory and DRAM), network architectures and overview of semiconductor technology & energy/power.

- EC571 (Digital VLSI Circuit Design) - *Spring 2010, Spring 2013, Fall 2013, Fall 2014, Fall 2015*
  The goal of this course is to expose students to various concepts of digital CMOS design. Starting with MOSFET basics, the course covers the design of combinational/sequential logic using static and dynamic CMOS design, the design of different types of CMOS-based memory arrays and the design of on-chip RLC interconnects. The theoretical concepts covered in class are consolidated through extensive CAD laboratory sessions. By the end of the course, the student are able to design a digital CMOS circuit to given area, power and performance specifications.

- EC700 (Advanced Computer Architecture) – *Spring 2019*
  The goal of this course is to learn the recent advancements in the area of computer architecture through lectures, reviewing research papers, and completing research-focused architecture design projects. We will focus on advanced single-core processor architectures, cache/memory architectures, on-chip net- work architectures and multicore processor architectures.

- EC772 (VLSI Graduate Design Project) - *Spring 2011*
  The goal of this course is to give students hands-on experience with designing digital CMOS chips. The design process includes design specifications, circuit/micro-architecture design, Verilog programming, chip floorplanning, placement and routing, parasitic extraction and validation. Students work in groups, and successful projects have the option of fabricating and testing their digital CMOS chips.

Department Service

- BU University Council Committee on Undergraduate Academic Programs & Policies Fall 2019 – Spring 2021
- BU Undergraduate Research Opportunities Program (UROP) Committee Spring 2016 – Spring 2017
- BU ECE Faculty Search Committee Fall 2016 – Spring 2017 (Member), Fall 2019 – Spring 2020 (Chair)
- BU Advising Network Fall 2015 – Spring 2017
- BU ENG Graduate Committee Spring 2015 – Spring 2017
- BU ECE Graduate Committee Fall 2009 – Spring 2017
- BU ECE Publicity Committee Fall 2009 – Spring 2017

Service on PhD Dissertation Committees

- Ashraf Al Daoud (Dissertation Defense in Fall 2009) - Committee Chair
- Marianne Nourzad (Dissertation Defense in Spring 2010) - Committee Chair
- Darin Hitchings (Dissertation Defense in Spring 2010) - Committee Chair
- Bharat Sukhwani (Dissertation Defense in Summer 2010) - Committee Chair
- Yirong Pu (Dissertation Defense in Fall 2010) - Committee Chair
- Zhen Wang (Dissertation Defense in Spring 2011) - 2nd Reader
- Ashfaq Khan (Prospectus Defense in Spring 2011, Dissertation Defense in Summer 2012) - 3rd Reader
- Jie Meng (Prospectus Defense in Fall 2011, Dissertation Defense in Summer 2013) - 3rd Reader
- Chen Chao (Prospectus Defense in Spring 2012, Dissertation Defense in Spring 2014) - PhD Advisor
- Min Huang (Dissertation Defense in Spring 2013) - Committee Chair
- Atabak Mahram (Dissertation Defense in Spring 2013) - Committee Chair
- Mahmoud Zangeneh (Prospectus Defense in Fall 2013, Dissertation Defense in Spring 2015) - PhD Advisor
- Can Hankendi (Prospectus Defense in Fall 2013, Dissertation Defense in Summer 2015) - 2nd Reader
- Schuyler Eldridge (Prospectus Defense in Spring 2014, Dissertation Defense in Summer 2016) - PhD Advisor
- Abdulkadir Yurt (Dissertation Defense in Summer 2014, Dissertation Defense in Summer 2014) - Committee Chair
- Tenzile Berkin Cilingiroglu (Dissertation Defense in Summer 2014) - 5th Reader
- Aydan Uyar (Prospectus Defense in Fall 2014, Dissertation Defense in Summer 2015) - 2nd Reader
- Hari Prasad Paudel (Dissertation Defense in Summer 2015) - Committee Chair
- Fulya Kaplan (Prospectus Defense in Fall 2015, Dissertation Defense in Spring 2017) – 2nd Reader
- Tiansheng Zhang (Prospectus Defense in Fall 2015, Dissertation Defense in Fall 2016) – 2nd Reader
- Zafar Takhirov (Prospectus Defense in Spring 2016, Dissertation Defense in Summer 2017) – PhD Advisor
- Ryan Silva (Prospectus Defense in Summer 2016, Dissertation Defense in Summer 2017) – 2nd Reader
- Amir Kavyani Ziabari (Northeastern Univ) (Prospectus Defense in Summer 2016, Dissertation Defense in Fall 2016) – 2nd Reader
- Boyou Zhou (Prospectus Defense in Spring 2017, Dissertation Defense in Spring 2019) – PhD Advisor
- Yenai Ma (Prospectus Defense in Spring 2018, Dissertation Defense in Summer 2020) – PhD Advisor
- Leila Delshadtehrani (Prospectus Defense in Summer 2018) – PhD Advisor
- Chen Yang (Prospectus Defense in Fall 2018) – 2nd Reader
- Saiful Mojumder (Prospectus Defense in Fall 2018) – PhD Advisor
- Onur Shahin (Dissertation Defense in Summer 2019) – 4th Reader
- Furkan Eris (Prospectus Defense in Fall 2019) – PhD Advisor
- Aditya Narayan (Prospectus Defense in Fall 2019) – 2nd Reader
- Marcia Sahaya Louis (Prospectus Defense in Fall 2019) – PhD Advisor
- Radhakrishna Sanka (Prospectus Defense in Summer 2020) – 2nd Reader
- Zihao Yuan (Prospectus Defense in Fall 2020) – 2nd Reader

Service on MS Thesis Committees

- Huaxin Dai (Thesis Defense in Spring 2010) - 2nd Reader
- Florian Raudies (Thesis Defense in Summer 2014) - MS Advisor
- Jeffrey Little (Thesis Defense in Fall 2014) - MS Advisor
- Anmol Gupta (Thesis Defense in Summer 2017) – MS Co-Advisor
- Vaibhav Bansal (Thesis Defense in Spring 2020) – 2nd Reader

Industry Experience

Google Inc. – *Sunnyvale, CA (August 2017 – August 2018)*
Classified Project

Intel Corporation **-** *Santa Clara, CA (May 2003 – Nov. 2003)*
Development of system validation tools for IA-64 family of processors

- Worked as a co-op in the Post Silicon Validation Dept. Designed and implemented two system debug tools (Trace Porter – bug transported from system level to tester (IMS) level for detailed analysis and Microarchitecture Analyzer – dump out data stored in cache and various registers during system failure to perform a cycle-accurate analysis) using assembly language programming, C and Perl for IA-64 family of processors.