DESIGNING MEMORY AND LOGIC CIRCUITS USING
HYBRID CMOS/MEMRISTOR TECHNOLOGY

by

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ABSTRACT

Memristor technology is being explored as a potential candidate in designing non-volatile memory arrays and logic circuits with high density, low latency and small energy consumption. In this thesis, we present the detailed functionality of multi-bit 1-Transistor 1-memRistor (1T1R) cell-based memory arrays, and propose possible applications of memristor devices for designing low-energy logic circuits in sub-threshold regime. We develop performance and energy models for an individual 1T1R memory cell and the memory array as a whole. We consider TiO$_2$- and HfO$_x$-based memristors, and for these technologies there is a sub-10% difference between energy and performance computed using our models and HSPICE simulations. Using a performance-driven design approach, the energy-optimized TiO$_2$-based RRAM array consumes the least write energy (4.06 pJ/bit) and read energy (188 fJ/bit) when storing 3 bits/cell for 100 nsec write and 1 nsec read access times. Similarly, HfO$_x$-based RRAM array consumes the least write energy (365 fJ/bit) and read energy (173 fJ/bit) when storing 3 bits/cell for 1 nsec write and 200 nsec read access times. On the logic side, we propose the use of memristors in the design of feedback equalizer circuits for digital logic circuits. We first propose the use of a variable threshold feedback equalizer circuit with combinational logic blocks to mitigate the timing errors in digital logic designed in sub-threshold regime. This mitigation of timing errors can be leveraged to reduce the dominant leakage energy by scaling supply voltage or decreasing the propagation delay. At the fixed supply voltage, we can decrease the propagation delay of the critical path in a combinational logic block using equalizer circuits and, correspondingly decrease the leakage energy consumption. For a 8-bit carry lookahead adder designed in UMC 130 nm process, the operating frequency can be increased by 22.87% (on average), while reducing the leakage energy by 22.6% (on average) in the sub-threshold regime. Overall, the feedback equalization technique provides up to 35.4% lower energy-delay product compared to the conventional non-equalized logic. For a 8-bit carry lookahead adder, the proposed error mitigation technique enables us to reduce the critical voltage (beyond which timing errors occur) from 300 mV (nominal design) to 270 mV (design with feedback circuit), and provides a 16.72% decrease in energy per operation when operating at the same frequency. In the next year, we will explore the design of a memristor-based feedback equalization technique to decrease the area/leakage overhead of the equalizer and explore any opportunities to dynamically
adjust the feedback strength and tune the designed sub-threshold logic circuit to achieve performance, energy and error rate specifications.
Contents

1 Introduction ................................................................. 1
   1.1 Background and Motivation ......................................... 1
   1.2 Completed Research and Future Work ............................ 3

2 Memristor Technology and Modeling ................................ 6
   2.1 Introduction ....................................................... 6
   2.2 Memristor Device Technology .................................... 6
   2.3 Summary .......................................................... 11

3 Design of Multi-bit RRAM Array .................................... 12
   3.1 Introduction ....................................................... 12
   3.2 Related Work ..................................................... 12
   3.3 RRAM Cell Design ............................................... 13
   3.4 RRAM Array Architecture ....................................... 14
   3.5 Performance Models ............................................. 16
   3.6 Energy Models ................................................... 23
   3.7 Memory Technology Comparison ................................ 27
   3.8 PVT Variation Analysis of n-bit RRAM Cell .................... 28
   3.9 Summary .......................................................... 34

4 Sub-threshold Logic Design using Feedback Equalization ........ 35
   4.1 Introduction ....................................................... 35
   4.2 Related Work ..................................................... 35
   4.3 Equalized Flip flop versus Conventional Flip flop .......... 36
   4.4 Experimental Results ............................................ 40
      4.4.1 Performance improvement at the fixed supply voltage .. 40
      4.4.2 Leakage reduction at the fixed operating frequency ... 42
      4.4.3 Mitigating process variations ............................ 43
   4.5 Effect of Technology Scaling ................................... 44
   4.6 Summary .......................................................... 45

5 Future Work .............................................................. 46

References ................................................................. 48
Chapter 1

Introduction

1.1 Background and Motivation

The design of fast and low-energy memory and logic circuits is a critical part of designing VLSI chips that are extensively used today in applications ranging from biomedical implants to handheld devices to laptops/desktops to large data centers. The performance, area and energy of most computer systems is increasingly limited by the capacity, access latency and energy consumption of on-chip memory blocks in today’s computing systems. The design of on-chip memory necessitates the integration of the memory with the processor in the same die. However, in this case the size of the die limits the storage capacity of the memory block. Furthermore, most modern mobile applications require the use of nonvolatile memory that enables switching off the power supply to suppress the amount of dynamic and static power components of the digital VLSI chips. Therefore, considering the limited available area, the access latency and the energy overhead for the design of on-chip memory blocks, it is necessary to explore emerging technologies and alternate circuit-level solutions which are compatible with the conventional CMOS process for designing highly-dense memory arrays.

1-Transistor 1-memRistor (1T1R) cell based resistive random access memory (RRAM) arrays have low access latency, low access energy and large density (that can allow us to fit the entire working set of an application on the processor chip). This research addresses the use of recently-explored memristor (RRAM) technology to design dense nonvolatile on-chip memory arrays for today’s computer architectures.

Table 1.1 shows a head-to-head comparison of the various nonvolatile emerging technologies. Each technology has its pros and cons, which has made it difficult to identify a successor to CMOS technology. Among these technologies, PCRAM requires large energy for its resistive switching behavior, FeRAM suffers from signal degradation in scaling process and MRAM has high endurance but it scales poorly and consumes large power due to large write currents. Among these emerging memory technologies, RRAM has been demonstrated with excellent high density capability due to multi-level cells (MLC) and cross-point array structures. RRAM technology (memristor) has also simple structure, high resistance ratio, fast-switching operation and device scalability beyond 10 nm technology node (Chiu et al., 2012). HP Labs has already announced plans to commercialize memristor-based RAM and predicted that RRAM could eventually replace traditional memory technologies. Therefore, the two-terminal memristor devices have been well-accepted as storage elements and are considered viable replacements to conventional CMOS-based memory designs. The
memristor can be considered as a variable resistor which can be programmed by changing the voltage drop across the memristor or changing the current injected into the memristor. Here, programming amounts to changing the value of the memristance which leads to two different states for the memristor. These two states can correspond to storage of logic 0 and logic 1 in the memristor.

The memristor technology can also be used in designing low-energy logic circuits. Although historically higher performance has been the main motivation behind the CMOS scaling process, speed is not the ultimate goal for all modern applications of integrated circuits (ICs). Instead, a wide class of applications are emerging for which power and more importantly energy is the main problem. Ultra-low power sub-threshold circuits are becoming prominent in emerging embedded applications including portable devices such as cell phones and cameras. Other emerging applications such as wireless sensor networks and medical instruments have low energy operation as the main constraint instead of performance.

Scaling supply voltage into the sub-threshold region significantly reduces the dynamic energy consumed by digital circuits. Scaling the supply voltage also lowers down the leakage current due to reduction in the drain induced barrier lowering (DIBL) effect resulting in considerable lower leakage power. Other techniques such as adaptive body biasing also enable threshold voltage adjustment and power tuning in the designed digital circuits. However, as the supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases enormously leading to the rise in leakage energy of the active devices operating in sub-threshold regime as the leakage power integrates over a longer period of time. As we scale the supply voltage, the two opposite trends in the leakage and the dynamic energy components lead to a minimum energy supply voltage and it has been shown in (Wang and Chandrakasan, 2005) that the minimum energy supply voltage of digital circuits occurs below the threshold voltage of the transistors.

Sub-threshold digital circuits, however, suffer from the degraded $I_{ON}/I_{OFF}$ ratios resulting in a failure in providing rail-to-rail output swings when restricted by aggressive timing constraints. Moreover, circuits working in weak inversion region suffer from process variations that directly affect the threshold voltage, which in turn has a significant impact on the

<table>
<thead>
<tr>
<th>Memory type</th>
<th>PCRAM</th>
<th>MRAM</th>
<th>FeRAM</th>
<th>RRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell</td>
<td>1T1R</td>
<td>1T1R</td>
<td>1T1C</td>
<td>1T1R</td>
</tr>
<tr>
<td>R/W time (nsec)</td>
<td>76/20e3</td>
<td>12</td>
<td>200/134</td>
<td>8.5/10</td>
</tr>
<tr>
<td>R/W energy ($\frac{J}{bit}$)</td>
<td>15.3</td>
<td>0.9/1.3</td>
<td>9.77</td>
<td>-</td>
</tr>
<tr>
<td>Endurance</td>
<td>$10^7$</td>
<td>$10^{16}$</td>
<td>$10^{13}$</td>
<td>$10^8$</td>
</tr>
<tr>
<td>Retention</td>
<td>$&gt;10$ yrs</td>
<td>$&gt;10$ yrs</td>
<td>$&gt;10$ yrs</td>
<td>$&gt;10$ yrs</td>
</tr>
<tr>
<td>Density ($\frac{Mb}{mm^2}$)</td>
<td>15.7</td>
<td>0.35</td>
<td>0.93</td>
<td>6.66</td>
</tr>
<tr>
<td>Tech. node (nm)</td>
<td>58</td>
<td>90</td>
<td>130</td>
<td>180</td>
</tr>
</tbody>
</table>

Table 1.1: Comparison between current emerging nonvolatile memory technologies.
drive current due to the exponential relationship between the drive current and the threshold voltage ($V_T$) of the transistors in sub-threshold regime. These degraded $I_{on}/I_{off}$ ratios and process-related variations thus make sub-threshold circuits highly susceptible to timing errors which can further lead to complete system failures. Since the standard deviation of $V_T$ varies inversely with the square root of the channel area (Pelgrom et al., 1989), one common approach to overcome the process variation is to upsize the transistors (Kwong et al., 2009). Increasing the logic path depth to leverage the statistical averaging of the delay across gates has been proposed in (Verma et al., 2008) to overcome process variations. A similar approach of choosing transistor sizes and logic depths that mitigate the impact of process variations has been proposed in (Zhai et al., 2005). Similarly, (Choi et al., 2004) proposes using gates of different drive strengths to overcome process variations. However, this increases the transistor parasitics, which in turn increases the energy consumption. Body-biasing approaches have also been proposed to mitigate the impact of variations in (Jayakumar and Khatri, 2005) and (Liu et al., 2011). Therefore, alternate circuit-level approaches are required to alleviate the timing errors while minimizing the energy consumption of the circuit.

1.2 Completed Research and Future Work

We analyzed the use of two-port memristor technology as potential storage element and present the design and optimization of low-power high-performance multi-bit 1T1R RRAM arrays. In addition, we improved the sub-threshold design of digital circuits by using a new feedback-based technique for mitigating timing errors in weak inversion region. The summary of the completed research of this thesis is as follows:

- We developed the performance and energy models for the read and write operation of a n-bit 1T1R RRAM cell designed using $TiO_2$ and $HfO_x$-based memristors. These performance and energy models were validated against HSPICE simulations, and for both $TiO_2$ and $HfO_x$ RRAM technologies there is a sub-10% difference between energy and performance computed using our models and HSPICE simulations. As part of the modeling effort, we also developed a SPICE model for $HfO_x$-based memristors.

- We designed and optimized the multi-bit 1T1R RRAM arrays with $TiO_2$ and $HfO_x$-based memristors, and we calculated the optimum number of bits/cell considering energy and performance constraints of the entire multi-bit RRAM array.

- We proposed a mechanism for read reliability optimization in multi-bit RRAMs where the read noise margin is maximized using non-uniform memristor state assignment. We compared the read and write energy consumption of multi-bit RRAM cells considering both non-uniform and conventional uniform memristor state assignments. Using the proposed performance and energy models, we presented a detailed analysis of the impact of process (P), voltage (V) and temperature (T) variations on the access time,
energy consumption and reliability of multi-bit RRAM cells. We determined the optimal number of bits per 1T1R RRAM cell for both $TiO_2$ and $HfO_x$-based memristors that provides reliable operation under PVT variations.

- We developed a new feedback equalizer circuit in sub-threshold regime that adjusts the switching thresholds of the gates just before the flip flops based on the prior sampled outputs and reduces the propagation delay of the critical path in the combinational logic block. This feedback equalizer circuit enables fast charging/discharging of the load capacitance of the critical path, which creates opportunities for increasing the operating frequency of the circuit and/or voltage scaling. These opportunities can be harnessed to reduce the circuit’s leakage energy - the dominant energy component in sub-threshold regime and improve the circuits robustness.

- We explored the leakage energy reduction when applying the feedback equalization technique using the following approaches: a) Reduce the propagation delay of the critical path using the feedback equalizer circuit and run the adder at a higher frequency to reduce dominant leakage energy. This reduces the energy-delay product of the digital logic circuit. b) Use the feedback equalizer to operate the circuit at the same frequency as the baseline but using a lower supply voltage and in turn lower leakage energy. c) Use feedback equalizer to mitigate the impact of process variations and avoid the need for oversizing the transistors in turn reducing the leakage energy.

- We also completed a detailed analysis of the effect of technology scaling on the use of feedback equalizer circuits for improving performance and reducing leakage energy of circuits operating in the sub-threshold regime.

Our future work includes the design of a memristor-based feedback equalization technique to decrease the area/leakage overhead of the equalized flip flop and provide the opportunity to dynamically adjust the feedback strength and tune the overall sequential logic block with respect to performance, energy and error rate constraints. The tunability of the feedback strength is possible by tuning the memristance value for the RRAM component of the feedback topology. The tasks that will be completed as part of the future work are as follows:

- We will design and optimize a CMOS-based adaptive equalizer circuit topology having various feedback strengths to dynamically tune the designed digital logic and meet the required performance constraints for a energy and error rate budget.

- We will develop memristor-based feedback equalizer circuit as a replacement to the CMOS-based feedback equalizer circuits.

- We will model the performance, energy and error rate of the proposed memristor-based feedback equalizer circuit.

- A detailed analysis of the destructiveness of the memristance value will be completed to ensure the correct functionality of the proposed memristor-based feedback equalization technique.
• We will design the required peripheral circuitry for programming the equalizer circuit and its corresponding overhead with respect to the entire logic design.

• We will compare the memristor-based feedback equalizer circuit with the conventional CMOS-based feedback equalizer circuit in terms of power, performance and area.

The rest of this document is organized as follows: In Chapter 2, we describe the device-level behavioral modeling of memristor technology. In Chapter 3, we propose performance and energy models for multi-bit RRAM array architectures, determine the optimal number of bits per RRAM cell and explore the effects of PVT variations on the functionality of multi-bit RRAM array architectures. In Chapter 4, we discuss the feedback equalization technique in ultra low-power sub-threshold digital circuits. In Chapter 5, we discuss our planned efforts for designing the adaptive memristor-based feedback equalization technique for sub-threshold digital logic circuits.
Chapter 2

Memristor Technology and Modeling

2.1 Introduction

Memristor is a two-terminal nanodevice that has been recently analyzed for its potential applications in memory design and logic design of both traditional and neuromorphic computing systems. It is a relatively well-explored device in terms of modeling, design methodology and its physical switching mechanism between two or more stable states. This chapter summarizes the current efforts on design and modeling of memristor devices and then explains the detailed functionality of our target $TiO_2$ and $HfO_x$-based memristors. A new state function that we developed for $HfO_x$-based memristor devices is also presented in this chapter.

2.2 Memristor Device Technology

Memristors provide a functional relationship between the charge and flux which was first postulated in (Chua, 1971). Several oxide-based memristor devices have been proposed as storage elements in the design of RRAM arrays. $HfO_x$ and $TaO_x$ have been widely used as switching elements in RRAM cells (Chen et al., 2009b), (Chen et al., 2009a), and (Lee et al., 2011). Although several fabricated RRAM prototypes based on different switching materials have been reported in the literature, only a few reliable device models have been proposed for large-scale circuit-level simulations (Ielmini, 2011), (Bersuker et al., 2011), and (Lu et al., 2011). A numerical model of filament growth based on thermally activated ion migration, which accounts for the resistance switching characteristics is proposed in (Ielmini, 2011). This model (primarily developed for $HfO_x$-based 1T1R cell) matches the measurement results for different metal oxide RRAM configurations ($HfO_x/ZrO_x$, $NiO$). The authors in (Guan et al., 2012a) analyze the variation of switching parameters in RRAM devices using a trap-assisted-tunneling (TAT) current solver considering the stochastic generation and recombination of oxygen vacancies. The compact model for the proposed RRAM switching behavior in (Guan et al., 2012a) is introduced in (Guan et al., 2012b), while the measurement results of the $HfO_x$-based prototypes verify this model in (Yu et al., 2012).

There are multiple efforts in place to develop accurate analytical and SPICE models for the two-terminal memristor elements (Pickett et al., 2009), (Zangeneh and Joshi, 2012), (Ielmini, 2011). An analytical $TiO_2$ memristor model and the corresponding SPICE code that express both the static transport tunneling gap width and the dynamic behavior of the memristor state based on the measurement results are proposed in (Pickett et al., 2009)
Figure 2.1: Physical structure of (a) TiO$_2$-based memristor between 2 Pt contacts consisting of a highly conductive doped region and a highly resistive undoped region, where $L =$ thickness of the memristor and $W =$ thickness of the conductive region, and (b) HfO$_x$-based memristor showing conductive filament growth/narrowing process where $\phi_{\text{min}}$ and $\phi_{\text{max}}$ are the minimum and maximum filament diameters, respectively.

The TiO$_2$-based memristor was first fabricated by HP (Strukov et al., 2008). The fabricated prototype had a highly resistive thin layer of TiO$_2$ and a second conductive deoxygenized TiO$_{2-x}$ layer (see Figure 2.1a). The change in the oxygen vacancies due to a voltage applied across the memristor modulated the dimension of the conductive region in the memristor. This resulted in a high resistance state and a low resistance state corresponding to the resistive and conductive region of operation, respectively. The effective ‘memristance’ of the memristor device can be calculated using Equation (2.1) (proposed in (Strukov et al., 2008)).

$$M(t) = R_{\text{ON}}x(t) + R_{\text{OFF}}(1 - x(t)).$$  \hspace{1cm} (2.1)

Here, $R_{\text{ON}}$ and $R_{\text{OFF}}$ are the minimum and maximum memristances, respectively, and $x(t)$
<table>
<thead>
<tr>
<th>Parameter</th>
<th>$TiO_2$</th>
<th>$HfO_x$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ON}(\Omega)$</td>
<td>100</td>
<td>3K</td>
</tr>
<tr>
<td>$R_{OFF}(\Omega)$</td>
<td>16K</td>
<td>10M</td>
</tr>
<tr>
<td>$L(\text{nm})$</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>$E_{A0}(eV)$</td>
<td>-</td>
<td>1.2</td>
</tr>
<tr>
<td>$A(ms^{-1})$</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>-</td>
<td>0.3</td>
</tr>
<tr>
<td>$\rho(\mu\Omega cm)$</td>
<td>-</td>
<td>400</td>
</tr>
<tr>
<td>$k_{th}(W m^{-1} K^{-1})$</td>
<td>-</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 2.1: Parameters of $TiO_2$-based (Strukov et al., 2008) and $HfO_x$-based (Ielmini, 2011), (Sheu et al., 2009) memristors used for modeling and simulations.

is the state of the memristor (Eshraghian et al., 2011) (see Figure 2.2). This state of the memristor can be calculated as $w(t)/L$, where $w(t)$ is the thickness of the conductive doped region as a function of time, and $L$ is the memristor thickness.

The rate of change of the memristor state follows the ionic drift model which is a function of the memristor physical parameters and the current through the memristor. As the current itself varies with time, the change of memristor state exhibits nonlinear behavior. This nonlinear behavior can be expressed using a window function shown in Equation (2.2) (Eshraghian et al., 2011).

$$\frac{dx}{dt} = \frac{\mu_v R_{ON}}{L^2} i(t) F(x(t), p) \quad (2.2)$$

In Equation (2.2), $\mu_v \approx 3 \times 10^{-8} m^2/s/V$ (Witrisal, 2009) is the average dopant mobility, $F(x(t), p)$ is the window function, where the parameter $p$ controls the memristor nonlinearity. Increasing $p$ yields a flat window function for larger memristor states. Window functions that consider the linear ionic drift, and the nonlinear behavior that appears at the boundaries of the memristor state, have been proposed in (Benderli and Wey, 2009) and (Joglekar and Wolf, 2009). However, both these window functions get stuck at the memristor state boundaries. We use the window function proposed in (Biolek et al., 2009) for developing the performance and energy models of the $TiO_2$-based RRAM cell. This function models the nonlinear behavior of the rate of change of state without getting stuck at the
Figure 2-3: Dynamic window function of the memristor state showing the non-linear behavior of the memristor for different control parameter $p$. The current sign function prevents the state from getting stuck at the two boundaries.

The window function is given by

$$F(x(t), p) = 1 - (x - \text{sgn}(-i(t)))^{2p}$$  \hspace{1cm} (2.3)

Here, $i(t)$ is the current through the memristor, $\text{sgn}$ is a sign function that prevents the state of the cell from getting stuck at the borders and $p$ is the control parameter. Figure 2-3 shows a plot of the window function for different $p$ values.

In case of the $HfO_x$-based memristor, the set/reset (changing memristor resistance to $R_{\text{ON}}/R_{\text{OFF}}$) process is performed by increasing/decreasing the diameter of the conductive filament (CF) using positively charged oxygen vacancies ($V_O$) or $Hf$ ions migration in a thermally activated hopping process in the filament growth model (Ielmini, 2011). Applying a voltage across the $HfO_x$-based memristor forces the positive ions to move along the direction of the electric field while increasing the maximum temperature along the CF and changing the effective cross section diameter of the CF (see Figure 2-1b). This rate of change of diameter was derived in (Ielmini, 2011) and is given by

$$\frac{d\phi}{dt} = Ae^{-\frac{E_{A0} - \alpha qV}{k T_0 \left[1 + \frac{q V^2}{\pi \rho k t_h} \right]}}$$  \hspace{1cm} (2.4)

where, $\phi$ is the CF diameter, $A$ is a pre-exponential constant, $E_{A0}$ is the energy barrier for ion hopping, $\alpha$ is the barrier lowering coefficient, $q$ is the elementary charge, $V$ is the applied voltage across the memristor, $k$ is the Boltzmann constant, $T_0$ is the room temperature, $\rho$ is the electrical resistivity and $k_{th}$ is the thermal conductivity. A similar expression with a negative rate of change is used for modeling the reset process in $HfO_x$-based memristors.

As voltage is applied across the $HfO_x$-based memristor, its cross section area changes and the instantaneous resistance of the CF changes according to $R(t) = 4\rho L / \pi \phi(t)^2$. The rate of change of the diameter for $HfO_x$-based memristors in filament growth model for set and reset operations is shown in Figure 2-4. The nominal parameter values of the memristor used for generating this plot are listed in Table 2.1. To minimize the destruction of the stored data during read operation, we maintain the voltage across the memristor to be greater than
Figure 2.4: Rate of diameter change for HfO$_x$-based memristors in filament growth model (Ielmini, 2011) for set (V > 0) and reset (V < 0) operations as a function of voltage across the memristor.

-1.7 V. Similarly, during write operation we maintain the applied voltage between 1 V to 4 V to minimize the set operation time.

To find the instantaneous memristance of the HfO$_x$ RRAM, we define a new state function for HfO$_x$ memristors as in Equation (2.5).

\[
x(t) = C \left(1 - \frac{\phi_{\text{min}}^2}{\phi(t)^2}\right)
\]  

(2.5)

where the coefficient C is

\[
C = \frac{\phi_{\text{max}}^2}{\phi_{\text{max}}^2 - \phi_{\text{min}}^2} = (1 - 1/\beta)
\]  

(2.6)

Here, \(\phi_{\text{max}}\) and \(\phi_{\text{min}}\) are the maximum and minimum CF diameters corresponding to \(R_{\text{ON}}\) and \(R_{\text{OFF}}\), and \(\beta = R_{\text{OFF}}/R_{\text{ON}}\). This state function can be plugged into equation (2.1) to calculate the effective memristance. Considering the rate of change of the CF diameter in (2.4) and the state function in (2.5), we define the rate of change of the HfO$_x$-based memristor state in Equation (2.7).

\[
\frac{dx}{dt} = \frac{2C\sqrt{(1-x/C)^3}}{\phi_{\text{min}}} \frac{d\phi}{dt}.
\]  

(2.7)

The corresponding HSPICE netlist that we developed for HfO$_x$-based memristors is:

```
.SUBCKT memristorHfOx PLUS MINUS phi
.PARAM phimin='sqrt((4*ro*L)/(3.14*Roff))'
.PARAM phimax='sqrt((4*ro*L)/(3.14*Ron))'
.PARAM C='phimax*phimax/(phimax*phimax- phimin*phimin)'
Csv phi 0 1
.IC V(phi) 0.3
Emem PLUS AUX VOL='I(Emem)*(V(phi)*Ron+ (1-V(phi))*Roff)'
```

10
The rate of change of the $HfO_x$-based memristor state is modeled as a voltage-controlled current source, and the combination of $sgn$ functions guarantees the reliable set/reset operations, and the normalized memristor state does not get stuck when approaching 1 or 0.

### 2.3 Summary

In this chapter, we first described the behavioral functionality of the $TiO_2$ memristor based on the ionic drift model. We then proposed the state function for the $HfO_x$-based memristors. A new reliable SPICE netlist for $HfO_x$ memristors was proposed based on the change in the conductive filament diameter.
Chapter 3

Design of Multi-bit RRAM Array

3.1 Introduction

In Chapter 2 we provided a detailed description of the memristor technology. In this chapter we provide a detailed discussion of the functionality of an n-bit 1T1R RRAM cell followed by a description of the architecture of a memory array designed using this RRAM cell as the building block. We discuss the implementation of memory cells and arrays using both TiO$_2$ and HfO$_x$-based memristors. We also discuss our performance and energy models for the n-bit 1T1R memory arrays designed using TiO$_2$- and HfO$_x$-based memristors.

3.2 Related Work

Several memory circuit/architecture topologies have been proposed in the literature based on the memristive structures. The authors in (Jo et al., 2009) used a Si-based memristive system to fabricate high-density crossbar arrays with high yield and OFF/ON ratio. A memristor-based TiO$_2$ memory cell is introduced in (Ho et al., 2011) and its functionality is evaluated using system-level simulations. An energy-efficient dual-element TiO$_2$-based memory structure is proposed in (Niu et al., 2010a), in which each memory cell contains two memristors that store the complementary states. Similarly, a 2-bit storage memristive cell is proposed in (Manem and Rose, 2011). Both these multi-bit memory cells have large area. Content addressable memory (CAM) designed using TiO$_2$ memristors has been introduced in (Eshraghian et al., 2011). A memristor-based Look Up Table (LUT) design has been introduced in (Chen et al., 2012) to replace the SRAM-based FPGA design while achieving higher density. In (Fei et al., 2012), the functionality, performance and power of several CMOS/memristor based circuits with memory applications have been verified using a simulator based on a Modified Nodal Analysis. An analysis of the peripheral circuitry of the crossbar array architecture is presented in (Xu et al., 2011). A nonvolatile 8T2R SRAM cell that uses two HfO$_x$-based 1T1R cells along with the conventional 6T SRAM structure is introduced in (Chiu et al., 2012) for low power mobile applications. A bridge-like neural synaptic circuit with 5 TiO$_2$-based memristors which is capable of performing sign/weight setting and synaptic multiplication operations is introduced in (Kim et al., 2012b). A memristor emulator composed of the basic circuit-level elements is designed in (Kim et al., 2012a). The authors in (Liauw et al., 2012) presented a 3D-FPGA with stacked RRAM technology achieving lower energy-delay product (EDP) and smaller area compared to the conven-
tional 2D-FPGA design. In (Xue et al., 2012), the authors proposed adaptive write and read circuits for RRAM arrays to enhance yield and $\beta$ ratio while eliminating large power consumption rising from the resistance fluctuations.

Memristors are highly vulnerable to process variation and several authors have analyzed its impact on the functionality of the memristive structures. Line-Edge Roughness (LERs) caused by uncertainties in the process of lithography and etching (Jiang et al., 2009), Oxide Thickness Fluctuations (OTFs) caused during sputtering or atomic layer deposition, and Random Discrete Doping (RDDs), which leads to randomness in resistivity of the conductive as well as the resistive region of the memristor, are generally the main causes of process variations. The authors in (Niu et al., 2010b) have analyzed the effect of cross section area and oxide thickness variations on the memristor resistance. The authors in (Hu et al., 2011a) have analyzed the effect of LER and OTF on the state $x(t)$, the rate of change of state $dx(t)/dt$ and power dissipation variations of $TiO_2$-based memristor. Using an Error Correcting Code (ECC) design that is commonly used in conventional DRAM memory, the authors in (Niu et al., 2012) propose the detection and mitigation of errors rising from process variations in both MOS-based and crossbar memristive RRAM cells. The authors in (Sheu et al., 2011) have used a Parallel-Series Reference-Cell (PSRC) scheme to decrease the reference current fluctuations in 1T1R RRAM structure. Moreover, using a Process-Temperature-Aware Dynamic BL-bias (PTADB) circuit, they lower the read disturbance caused by bitline voltage variations.

We present the detailed energy and performance models of multi-level 1T1R RRAM cells that use $TiO_2$- and $HfO_x$-based memristors. For the $HfO_x$-based array design, we use the filament growth model in (Ielmini, 2011) that has been validated against measurement results. We determine the optimum number of bits per RRAM cell that consumes the least energy while being constrained by cell performance. We apply the Monte-Carlo methodology in (Hu et al., 2011a) to model the effects of LER, OTF and RDD on the functionality of multi-bit $HfO_x$ as well as $TiO_2$ RRAM cells.

### 3.3 RRAM Cell Design

The circuit of the 1T1R RRAM cell is similar to a DRAM cell and consists of an access transistor and a memristor as storage element (see Figure 3-1). Similar to DRAM, the access transistor is enabled for both read and write operations. As the memristor device shows considerable nonlinearity when approaching the states of 0 ($R_m = R_{OFF}$) and 1 ($R_m = R_{ON}$), it increases the required set/reset operation times at the two boundaries. We therefore ignore the states smaller than 0.1 and larger than 0.9 for faster set/reset i.e. write operations. The n bits of a cell are stored in the $2^n$ distinct sub-ranges in the range of 0.1 to 0.9. For an n-bit cell design, the state assignment can be done such that maximum noise margin would be achieved. For example, for a 2-bit RRAM cell, a memristor state below 0.3 corresponds to 00, a memristor state between 0.3 and 0.5 corresponds to 01, a memristor state between 0.5 and 0.7 corresponds to 11 and a memristor state above 0.7 corresponds to 10. We use Gray coding to increase the robustness and minimize the probability of getting two
Figure 3.1: 1-transistor 1-memristor (1T1R) RRAM cell.

bits in error in the read operation. We refer to this assignment as uniform state assignment. A non-uniform state assignment could also be used for the n-bit cell. A comparison of the two assignments is presented in Section 3.8.

To perform the read operation, the loadline is driven to charge the bitline through the memristor and access transistor. The read operation of the n-bit RRAM cell may be destructive and could require periodic refreshing of the cell data. For threshold-based memristor technologies recent measurement results have shown that if the drive voltage is less than a threshold, the state does not change for fast read operations (see Figure 2-4). The $\text{TiO}_2$ RRAM - based on the ionic drift model - is not a threshold-based technology (Kvatinsky et al., 2013) and shows more destructiveness during read cycles. A detailed analysis of the read destructiveness in multi-bit RRAM cells is proposed in Section 3.5.

The write operation always consists of two sub-operations – read followed by write as we need to know the data currently stored in the cell to determine the exact voltage that needs to be applied across the memristor to write new data. To perform the write operation, a positive or negative voltage is applied across the memristor for transitions to higher or lower states, respectively. The current flowing through the memristor changes the size of conductive region (in ionic drift model) or changes the diameter of the conductive filament (in filament growth model), thus increasing or decreasing the ‘memristance’. In the rest of the thesis, we refer to the memory read and write operations as $\text{read}_{\text{top}}$ and $\text{write}_{\text{top}}$, and the sub-operations as $\text{read}_{\text{sub}}$, $\text{refresh}_{\text{sub}}$ and $\text{write}_{\text{sub}}$. Thus $\text{read}_{\text{top}} = \text{read}_{\text{sub}} + \text{refresh}_{\text{sub}}$, while $\text{write}_{\text{top}} = \text{read}_{\text{sub}} + \text{write}_{\text{sub}}$.

3.4 RRAM Array Architecture

The overall architecture of a memory array built using 1T1R RRAM cells is similar to the conventional DRAM array i.e. a wordline is used to select a row of cells, and a bitline is
shared by the cells in a column for reading/writing (see Figure 3-2). In an RRAM array architecture, to perform the read sub operation, we first discharge the bitline (BL) to 0 \( V \), and then enable the wordline (WL) and loadline (LL) for a fixed predefined time. For the n-bit/cell array, when the WL and LL are enabled, the bitline charges to one of the \( 2^n \) distinct voltages corresponding to the \( 2^n \) distinct data values (i.e., the memristor state) stored in the cell. For instance in a 2-bit/cell array, there will be 4 distinct data values. An analog-to-digital converter (ADC) can be used to retrieve the n bits in each cell during the read operation. Each n-bit ADC consists of \( 2^n - 1 \) differential sense-amplifiers, each having the \( V_{BL} \) as one input and a unique reference voltage \( (V_{refi}) \) as the other input. For example a 2-bit/cell array needs 3 differential sense amplifiers. The \( 2^n - 1 \) sense amplifiers are shared by all the cells in the column. The sense amplifiers could be shared between columns to relax the area constraints on sense amplifier design. The rail-to-rail outputs of the sense amplifiers are fed to thermometer-to-binary code decoders that determine the exact data stored in the n-bit 1T1R cell and is given by bit \( B_{out}^0 \) to \( B_{out}^{n-1} \). We use the multiplexer-based decoder introduced in (Sail and Vesterbacka, 2004) which has a short critical path and consumes low power.

To perform the write sub operation, one of the \( 2^{2n} - 2^n \) different voltages (corresponding to the \( 2^n(2^n - 1) \) possible transitions for the n-bit RRAM cell) need to be applied across the memristor. For example, a 2-bit/cell array needs 12 voltages corresponding to 12 different transitions. The refresh sub operation would be similar to the write sub operation and the applied voltage will depend on the mechanism used for refresh operation. A 2n-bit multiplexer-based digital-to-analog converter (DAC) can be used to generate the voltages to be applied across the memristor for write sub/refresh sub operation. During write sub/refresh sub operation, the outputs \( B_{out}^0 \) and \( B_{out}^{n-1} \) are connected to the \( B_0^n \) and \( B_{n-1}^n \) inputs (corresponding to the current stored bits) and the data to be written into the cell is connected to the \( B_{out}^0 \) and \( B_{out}^{n-1} \) inputs of the 2n-bit DAC. This ensures the DAC generates the correct voltage to
be applied to the bitline for writing the data. For the 2-bit/cell array, we need a 4-bit DAC that generates 12 different set/reset voltages and an ADC with 3 sense amplifiers.

3.5 Performance Models

As discussed in Section 3.3, the read\textsubscript{top} and write\textsubscript{top} operation of the n-bit 1T1R cell consists of read\textsubscript{sub} + refresh\textsubscript{sub} and read\textsubscript{sub} + write\textsubscript{sub} operations, respectively. The equivalent circuit model for the 1T1R RRAM cell during read\textsubscript{sub} operation is shown in Figure 3-3. Here, $R_m$ is the equivalent time-variant resistance of the memristor and $R_{ch}$ is the access transistor channel resistance while operating in the triode region. The transmission gate which is part of the pre-discharging path of the bitline capacitor is not included here as that transmission gate is switched OFF as soon as BL is discharged resulting in very high equivalent resistance for the transmission gate. $C_{BL}$ and $C_d$ are the bitline capacitor and access transistor junction capacitor, respectively. Also $R_{BL}$ is the total resistance of the bitline. The bitline voltage at the end of read\textsubscript{sub} operation (i.e. after time $T_R$) will be

$$V_{BL} = V_{LL}(1 - e^{-(R_m(t)+R_{ch}+0.5R_{BL}/C_{BL})}). \quad (3.1)$$

Here the time constant of the junction capacitor ($C_d$) is much smaller than that of the bitline capacitor ($C_{BL}$), and hence $C_{BL} + C_d$ has been approximated to be equal to $C_{BL}$. Also, the term $0.5R_{BL}C_{BL}$ is the intrinsic time constant of the bitline modeled as a distributed RC-line. We assume the bitline, wordline and loadline to be 1 mm long, each with total capacitance of 200 fF and total resistance of 6.5 KΩ corresponding to copper metal line with 50 nm × 50 nm cross-section area. In addition, we assume the distributed RC-line model with 80 segments for all of the interconnects in the RRAM array architecture. For a n-bit RRAM cell, equation (3.1) can be used to define the $2^n - 1$ reference voltages to be input to the sense amplifiers that are used to differentiate between the different stored values while performing read\textsubscript{sub} operation. For example, for a 2-bit RRAM cell, we can use equation (3.1) to determine the three different reference voltages to differentiate between the four different stored values. The bitline voltage depends on the data stored in the memristor, i.e. the memristor state. For $V_{ref1} > V_{BL}$, $V_{ref1} < V_{BL} < V_{ref2}$, $V_{ref2} < V_{BL} < V_{ref3}$ and $V_{ref3} < V_{BL}$ the stored data is 00, 01, 11 and 10, respectively. In Table 3.1, we compare the reference voltages calculated using the analytical model shown in Equation (3.1) and using HSPICE simulation using 22 nm PTM technology (Ptm, ). The parameters of $TiO_2$ and $HfO_x$-based memristors that are used in modeling and HSPICE simulations are summarized

![Figure 3-3: Equivalent circuit of 1T1R cell for read\textsubscript{sub} (left) and write\textsubscript{sub}/refresh\textsubscript{sub} (right) operation.](image-url)
Table 3.1: Comparison between the reference voltages determined using analytical model (AM) and HSPICE simulation (HS) for a read sub access time of $T_{R}(TiO_2) = 1, 2$ nsec and $T_{R}(HfO_x) = 200, 400$ nsec in the 2-bit/cell 1T1R RRAM. $V_{LL}(TiO_2) = 0.48$ V and $V_{LL}(HfO_x) = 0.7$ V are chosen to reach to at least 25 mV difference between the two adjacent reference voltages. The average error is 5.7% for $TiO_2$ and 0.151% for $HfO_x$.

<table>
<thead>
<tr>
<th>Reference Voltages</th>
<th>AM $TiO_2$ 1 nsec</th>
<th>HS $TiO_2$ 1 nsec</th>
<th>AM $TiO_2$ 2 nsec</th>
<th>HS $TiO_2$ 2 nsec</th>
<th>AM $HfO_x$ 200 nsec</th>
<th>HS $HfO_x$ 200 nsec</th>
<th>AM $HfO_x$ 400 nsec</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ref1}$</td>
<td>137.5 mV</td>
<td>120.5 mV</td>
<td>162 mV</td>
<td>158.17 mV</td>
<td>94.5 mV</td>
<td>94.79 mV</td>
<td>100.85 mV</td>
</tr>
<tr>
<td>$V_{ref2}$</td>
<td>168 mV</td>
<td>153.5 mV</td>
<td>190.4 mV</td>
<td>188.69 mV</td>
<td>130.5 mV</td>
<td>130.9 mV</td>
<td>135.25 mV</td>
</tr>
<tr>
<td>$V_{ref3}$</td>
<td>215.5 mV</td>
<td>202.5 mV</td>
<td>228.9 mV</td>
<td>231.37 mV</td>
<td>214 mV</td>
<td>214.6 mV</td>
<td>204.8 mV</td>
</tr>
</tbody>
</table>

Figure 3-4: Bitline voltage of a 2-bit/cell $TiO_2$-based RRAM for different bitline voltage development times.

Figure 3-5: Bitline voltage of a 2-bit/cell $HfO_x$-based RRAM for different bitline voltage development times.

in Table 2.1. Here the read time of 1, 2 ns (for $TiO_2$) and 200, 400 ns (for $HfO_x$) is chosen based on the nominal $\beta$ value for the two types of memristors (see Table 2.1). $HfO_x$ has larger $\beta$ and $R_{OFF}$ values compared to $TiO_2$, and therefore it needs higher read time for reliable read operation. If we ignore the destructiveness (changing the memristance) during read sub in the analytical model for simplicity, the resulting average error is 5.7% for $TiO_2$ and 0.151% for $HfO_x$. 
To ensure a reliable read operation, there should be sufficient difference in the four different voltages developed on the bitline corresponding to the 4 different data that can be stored in the 2-bit cell. For very large bitline voltage development times, the bitline can get completely charged to the load line voltage ($V_{LL}$). At the same time, for very small bitline voltage development times, the difference in the bitline voltages may not be large enough for the sense-amplifiers to correctly determine the data stored in the cell. The bitline voltage of TiO$_2$- and HfO$_x$-based 2-bit/cell RRAM cells for various bitline voltage development times during read operation are shown in Figures 3·4 and 3·5, respectively. For our 2-bit/cell RRAM array example, we design our sense amplifier such that it needs at least 12.5 mV differential inputs. Hence, we need at least 25 mV difference between the adjacent bitline voltages corresponding to the 4 different data that can be stored in the 2-bit cell. The $V_{ref}$ inputs to the three sense amplifiers are chosen based on bitline voltages (corresponding to the four different data that can be stored in the cell) while ensuring the 12.5 mV differential input. So for the TiO$_2$- and HfO$_x$-based 2-bit/cell RRAM cells we choose bitline development time of 1 nsec and 200 nsec, respectively. In the TiO$_2$-based cell, for the 1 nsec read access time, the four different bitline voltages are 125 mV, 150 mV, 186 mV and 245 mV. The corresponding $V_{ref1}$, $V_{ref2}$ and $V_{ref3}$ values are 137.5 mV, 168 mV, and 215.5 mV, respectively. Similarly, in the HfO$_x$-based cell, for the 200 nsec read access time, the four different bitline voltages are 82 mV, 107 mV, 154 mV and 274 mV. The corresponding $V_{ref1}$, $V_{ref2}$ and $V_{ref3}$ values are 94.5 mV, 130.5 mV, and 214 mV, respectively. The read times as a function of number of bits/cell (n) is illustrated in Figure 3·6. These read times have been chosen using the same approach as described above for the 2 bits/cell RRAM cell. As the value of n increases, we need larger read times to ensure the reliable read operation.

As discussed in section 3.3, the read$_{sub}$ operation of the 1T1R cell can be destructive. The read destructiveness of TiO$_2$-based memristors is larger compared to HfO$_x$-based memristors for the same loadline voltage ($V_{LL}$). The TiO$_2$-based memristor therefore needs to be refreshed more frequently than HfO$_x$-based memristor. Considering the rate of change of state for TiO$_2$ RRAM in Equation (2.2), the number of consecutive read operations that will not destruct the stored data in multi-bit TiO$_2$-based 1T1R RRAM cell, i.e. the refresh
threshold can be written as (Zangeneh and Joshi, 2013)

\[ t_{ref-TiO_2} \approx \frac{(x_{max} - x_{min})(R_m(x) + R_ch)}{2^n \gamma T_{RLL} (1 - (x - 1)^{2p})}. \] (3.2)

Here, \( R_m(x) \) is the resistance of the memristor for each state, \( n \) is the number of bits/cell, \( T_R \) is the read access time, \( x_{max} \) and \( x_{min} \) are the maximum and minimum normalized memristor states (0.9 and 0.1 in this work), respectively and \( \gamma = \frac{\mu R_{ON}}{L^2} \). Large \( V_{LL}, n \) and \( R_{ON} \) values (smaller \( \beta \)) necessitate more frequent refresh operation in the multi-bit RRAM cell. The contour plots of the number of consecutive non-destructive read operations in multi-bit \( TiO_2 \) RRAM is shown in Figure 3-7 for different \( n \) (number of bits/cell) and \( V_{LL} \) values for a memristor with initial state of \( x = 0.9 \). In case of the highly destructive multi-bit \( TiO_2 \) memristor, we explored two different refresh schemes: A refresh operation can be performed after each read cycle to compensate for destructiveness (Niu et al., 2010b). In this refresh scheme, we apply a \(-V_{LL}\) for the same duration as \( read_{sub} \). This doubles the read energy and lowers the performance of the RRAM array. A second refresh approach is to use a counter to track the current state of the memristor as well as the number of consecutive read operations. A refresh operation is done once the number of consecutive read operations on the multi-bit \( TiO_2 \) RRAM cell exceeds the threshold. For instance, in a 3-bit/cell \( TiO_2 \)-based RRAM array with \( V_{LL} = 0.1 \) V, 50 consecutive read cycles will result in loss of data (see Figure 3-7), so a 6-bit counter will be required to track the magnitude of destructiveness and perform refresh operation. Although the counter-based refresh approach seems more beneficial in multi-bit \( TiO_2 \) RRAM compared to the read followed by refresh scheme, our analysis shows that the energy and area overhead of the counter-based approach makes it infeasible.

Considering the rate of change of state for \( HfO_2 \) RRAM in Equation (2.7), the number of consecutive non-destructive read operations in multi-bit \( HfO_2 \)-based 1T1R RRAM cell will be

\[ t_{ref-HfO_2} = \frac{\phi_{min}(x_{max} - x_{min})}{2^n + 1 T_R C \sqrt{(1 - x/C)^3} \frac{d\phi}{dt}}. \] (3.3)
Figure 3.8: Contour plots of the number of consecutive non-destructive read cycles in multi-bit $HfO_x$-based RRAM for different $n$ and $V_{LL}$ values ($x = 0.9$).

The corresponding contour plots of the number of consecutive non-destructive read operations for different $n$ and $V_{LL}$ values for a memristor with initial state of $x = 0.9$ is shown in Figure 3.8. The threshold-based conductive filament growth mechanism in $HfO_x$ memristor makes it more resilient to read destructiveness compared to ion-drift mechanism based $TiO_2$ memristors. As can be seen in Figure 3.8, for small read voltage values a large number of consecutive read operations are required to destruct the current state in multi-bit $HfO_x$ RRAM technology. The refresh threshold proposed in Equation (3.3) and shown in Figure 3.8 exceeds the maximum allowed number of accesses (endurance) in the $HfO_x$-based RRAMs reported in (Sheu et al., 2009) (see Table 1.1) and (Chiu et al., 2012) which practically makes $HfO_x$ a non-destructive memristor technology at small read voltages. In case large voltages are used for $read_{sub}$ operation, then we might observe destructiveness of memristor state. To combat this, we propose to use a counter that tracks the current state of the memristor as well as the number of consecutive read operations. A refresh operation is done once the number of read operations exceeds the threshold given by Equation (3.3).

The equivalent circuit model for the refresh$_{sub}$/write$_{sub}$ operation of a 1T1R RRAM cell is shown in Figure 3.3. For the $TiO_2$-based memristor the refresh$_{sub}$/write$_{sub}$ operation model uses the window function proposed in (Biolek et al., 2009). The switching time of the bitline capacitor and the junction capacitor are orders of magnitude lower than the switching time of the memristor. Hence, we do not consider these two capacitors in our analytical models. Given the threshold voltage ($V_{th}$) drop across the access transistor (i.e. $R_{ch}$), the expression for memristor current during refresh$_{sub}$/write$_{sub}$ operation is

$$i_w(t) = \frac{V_{BL} - V_{th} - V_{LL}}{R_m(t)}.$$  \hspace{1cm} (3.4)

Using the window function in Equation (2.3) and the rate of change of state in Equation (2.2), the refresh$_{sub}$/write$_{sub}$ time can be approximated as

$$T_W = \frac{R_{OFF}Q_i}{(V_{BL} - V_{LL} - V_{th})\gamma}.$$  \hspace{1cm} (3.5)
where $\gamma = \frac{\mu_v R_{ON}}{L^2}$. Here $Q_i = \int_{x_i}^{x_{i+1}} \frac{1-x}{x^4} \, dx$ is the nonlinear delay integral for transitions to higher memristor states where $x_i$ is the state of memristor and $Q_i = \int_{x_i}^{x_{i+1}} \frac{1-x}{(x-1)^4} \, dx$ is the nonlinear delay integral for transitions to lower memristor states (note that here $Q_i$ could be negative leading to a negative voltage across the memristor for transitions to lower states). Here the resistance of the memristor is approximated as $R_m(t) \approx R_{OFF}(1-x(t))$ for simplicity. The integrals are determined from the window function we considered previously to model the nonlinearity of the memristor at the boundaries in equation (2.3) with $p = 2$.

For the n-bit RRAM cell, the limits of the nonlinear delay integral $Q_i$ will change based on $2^n$ different states. As an example, for the 2-bit cell we compared the required bitline voltages for 12 possible write sub transitions for 100 ns and 200 ns time period in $TiO_2$-based 1T1R memory cells in Figure 3-9. The $V_{LL}$ voltage is maintained at 1.5 V for all transitions. The average error between the analytical model and the HSPICE simulation results for a 2-bit $TiO_2$-based 1T1R memory cell is 9.81%.

For the $HfO_x$-based memristor using the rate of change of state in (2.7), the set/reset time of the 1T1R RRAM cell can be modeled as

$$T_W = \frac{\phi_{\min}}{2C} \left( \frac{d\phi}{dt} \right)^{-1} U_i$$

(3.6)
where $U_i = \int_{x_i}^{x_{i+1}} \frac{dx}{\sqrt{(1-x/C)^3}}$ is the nonlinear delay integral for $HfO_x$-based memristors for transitions to higher states and $U_i = \int_{x_i}^{x_{i+1}} \frac{dx}{\sqrt{(1-x/C)^3}}$ is the nonlinear delay integral for $HfO_x$-based memristors for transitions to lower states. For the n-bit RRAM cell, the limits of the nonlinear delay integral $U_i$ will change based on $2^n$ different states. Similar to the $TiO_2$-based memristor, there is a threshold voltage drop across the access transistor for set operation. The $HfO_x$ cell write access time in (3.6) does not include the 0%-90% distributed $RC$-line transition time for bitline ($R_{BL}C_{BL}$) which will later be included in the whole RRAM array design specification. Comparing results from the analytical model and the HSPICE simulation for 1 ns and 2 ns time period for a 2-bit $HfO_x$-based 1T1R memory cell in Figure 3-9, the average error is 5.19%. The modeling error for $HfO_x$-based cell is different from the $TiO_2$-based cell due to the different electrical parameters for each type of cell (see Table 2.1).

The contour plots for the set time constraints of 2 bits/cell $TiO_2$-based and $HfO_x$-based RRAM is shown in Figure 3-10 and Figure 3-11. Write speed is limited by the voltage applied across the memristor ($V_{mem}$). The write operation of $HfO_x$-based memristor is faster compared to $TiO_2$-based due to the faster rate of change of state of $HfO_x$ memristors.
<table>
<thead>
<tr>
<th>Cell Data</th>
<th>AM $T_iO_2$</th>
<th>HS $T_iO_2$</th>
<th>AM $HfO_x$</th>
<th>HS $HfO_x$</th>
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</thead>
<tbody>
<tr>
<td>00</td>
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<tr>
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<td>23.57 fJ</td>
<td>26.48 fJ</td>
<td>38.47 fJ</td>
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</tr>
</tbody>
</table>

Table 3.2: Comparison between analytical model (AM) and HSPICE simulations (HS) for energy dissipated in the cell while reading 2-bit RRAM cell with a read access time of $T_R(T_iO_2) = 1\text{nsec}$ and $T_R(HfO_x) = 200\text{nsec}$. The average error is 8.44% and 0.038% for $T_iO_2$ and $HfO_x$ respectively.

3.6 Energy Models

In this section, we present the models for energy consumption during read$_{sub}$ and write$_{sub}$/refresh$_{sub}$ operation. It should be noted that the energy consumed in the wordline, bitline and loadline depends on the aspect ratio of the memory array. Once the array structure is finalized the energy can be determined based on bitline capacitance ($C_{BL}$), loadline capacitance ($C_{LL}$) and wordline capacitance ($C_{WL}$). The energy dissipated in the cell during read$_{sub}$ operation (for both $T_iO_2$ and $HfO_x$) can be expressed as

$$E_R = \int_{0}^{T_R} V_{LL} i_R(t) \, dt$$  \hspace{1cm} (3.7)

where $i_R(t)$ is the memristor current during the read$_{sub}$ operation. Using the RC circuit model in Figure 3-3, the energy dissipated in the n-bit RRAM cell at the end of read$_{sub}$ operation will be

$$E_R = C_{BL} V_{LL}^2 (1 - e^{-TR_{m(t)} + R_{ch} + 0.5 R_{BL} C_{BL}}).$$ \hspace{1cm} (3.8)

Table 3.2 compares the energy dissipation calculated from the analytical model and determined using HSPICE simulation during read$_{sub}$ operation of a 2-bit $T_iO_2$-based RRAM cell having a latency of 1 $\text{nsec}$ as well as a 2-bit $HfO_x$-based RRAM cell having a latency of 200 $\text{nsec}$ for different stored data values. The average error is 8.44% and 0.038% for $T_iO_2$ and $HfO_x$ respectively.

The read energy contour plots for different number of bits/cell for both $T_iO_2$- and $HfO_x$-based RRAMs are illustrated in Figure 3-12 and Figure 3-13. For each value of bits/cell and each read timing constraint, we find the $V_{LL}$ value that gives at least 25 mV difference between two adjacent reference voltages of the sense amplifiers for reliable read operation. The difference between the reference voltages of the sense amplifiers is determined by the offset voltage of the input transistors in the voltage sense amplifiers and could be further reduced by increasing area at the expense of power (Schinkel et al., 2007). Higher number of bits/cell requires larger drive voltages to increase read noise margin and therefore consumes
more energy during read operation. Larger read times require lower drive voltages and dissipate lower amount of energy.

The instantaneous current of the memristor while performing refresh\textsubscript{sub}/write\textsubscript{sub} operation in the $TiO_2$-based cell is determined by Equation (3.4). Considering the $V_{th}$ voltage drop across the access transistor, the energy dissipated in the cell during refresh\textsubscript{sub}/write\textsubscript{sub} operation can be calculated as

$$E_W = \frac{T_W}{\gamma} \int_0^T (V_{BL} - V_{th} - V_{LL})i_W(t) \, dt = \frac{(V_{BL} - V_{th} - V_{LL})P_i}{\gamma}$$

(3.9)

where $\int i_W(t) \, dt = P_i / \gamma$ and $P_i = \int_{x_i}^{x_{i+1}} \frac{dx}{1-x^4}$ is the nonlinear energy integral for transitions to higher memristor states and $P_i = \int_{x_i}^{x_{i+1}} \frac{dx}{1-(x-1)^4}$ is the nonlinear energy integral for transitions to lower memristor states. The dissipated energy in the diffusion capacitor of the access transistor is ignored since it’s much smaller than the overall cell energy. For the n-bit RRAM cell, the limits of the nonlinear energy integral $P_i$ will change based on $2^n$ different states.

Figure 3.9 compares the energy dissipated in a 2-bit 1T1R cell for write\textsubscript{sub} in 12 possible
Table 3.3: Transition times of different components in the multi-bit RRAM array.

<table>
<thead>
<tr>
<th>Component</th>
<th>Transition Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wordline</td>
<td>1.3 nsec</td>
</tr>
<tr>
<td>Loadline</td>
<td>1.3 nsec</td>
</tr>
<tr>
<td>ADC</td>
<td>1 nsec</td>
</tr>
<tr>
<td>Mux-based DAC</td>
<td>1 nsec</td>
</tr>
</tbody>
</table>

Transitions calculated using the analytical model and the HSPICE simulation for TiO$_2$-based configurations with transition time of $T_W = 100 \text{nsec}$ and $200 \text{nsec}$. The average error is 8.71%.

The write$_{\text{sub}}$/refresh$_{\text{sub}}$ energy in the HfO$_x$-based memristor is modeled as

$$E_W = \int_0^{T_W} \frac{V^2}{R(t)} dt$$

(3.10)

where $V$ is the voltage across the memristor. Here using $R(t) = (1 - x(t)/C)R_{\text{OFF}}$, the closed form expression for write$_{\text{sub}}$/refresh$_{\text{sub}}$ energy in n-bit 1T1R HfO$_x$-based cell is

$$E_W = V^2 \phi_{\text{min}} \left( \frac{d\phi}{dt} \right)^{-1} S_i$$

(3.11)

where $S_i = \int_{x_i}^{x_{i+1}} \frac{dx}{\sqrt{(1-x/C)^3}}$ is the nonlinear energy integral for HfO$_x$-based memristors. Since there is a threshold voltage drop across the access transistor, the write voltage ($V$) in (3.11) is chosen as one threshold voltage below the difference between $V_{\text{BL}}$ and $V_{\text{LL}}$ voltages. In the n-bit RRAM cell, the limits of the nonlinear energy integral $S_i$ will change based on $2^n$ different states. The average error between the dissipated energy of a 2-bit HfO$_x$ RRAM cell model and the simulation results is 5.25% (see Figure 3·9). We do not consider the effect of subthreshold leakage in our energy analysis since all transistors are working in strong-inversion region of operation.

Using the energy models, we compare the different energy components of the 1T1R RRAM array for different number of bits/cell. The transition times of different components (other than the cell) in the RRAM array have been assumed constant for different number of bits and are summarized in Table 3.3. The energy consumption in different components of the RRAM array during read operation for TiO$_2$-based RRAMs is illustrated in Figure 3·14. Cell energy increases during read operation for higher number of bits. This is due to higher loadline voltages required for providing sufficient read noise margin for higher number of bits/cell. Since the read process of multi-bit TiO$_2$ RRAM is destructive (see Figure 3·7), we consider the energy of read followed by a refresh operation in Figure 3·14. The total wordline energy is constant across all cells. The number of sense amplifiers increases with number of bits/cell ($2^n - 1$ sense amplifiers for n-bit RRAM cell), and so the energy/bit of the sense amplifiers increases. The same trend is observed for the decoder energy as the number of multiplexers increases with number of bits/cell.
To increase the read reliability of multi-bit RRAM array, we assume there should be at least 25 mV difference between two adjacent reference voltages. One way to reach this voltage difference is to use uniform state assignment and increase the $V_{LL}$ voltage. In the uniform state assignment scheme, there is a fixed distance between two adjacent states. Another way of reaching the 25 mV difference between two adjacent reference voltages is by lowering $V_{LL}$ voltages, and choosing the appropriate memristor states such that the read reliability would be maximized. This approach is called non-uniform state assignment where the 0.1 to 0.9 range for the state of a memristor is not uniformly shared between the 2^n different data that can be stored in the cell. Comparing uniform and non-uniform state assignment strategies, the non-uniform state assignment consumes lower energy due to lower $V_{LL}$ values. The minimum total read energy/operation is consumed at n=2 for uniform state assignment and n=3 for non-uniform state assignment. Considering the same throughput constraint (# bits/cell n=3) for both cases, non-uniform state assignment consumes 32.1% less energy than uniform state assignment.

Using the same approach, we show the energy consumption in different components of the RRAM array during read operation for $HfO_x$-based RRAMs using uniform and non-uniform state assignments in Figure 3·15. The refresh energy of the multi-bit $HfO_x$ memristor is
amortized across the different components of the array. Compared to TiO$_2$ and considering the same throughput constraint (n=3) the HfO$_x$ RRAM array using non-uniform state assignment has 59.07% lower total read energy consumption.

The energy consumed in the various components of the RRAM array during write operation for both TiO$_2$- and HfO$_x$-based RRAMs are shown in Figure 3·16 and Figure 3·17. Since the size of mux-based DAC increases with number of bits per RRAM cell, the energy consumption of the DAC increases accordingly. The total wordline and loadline energy is constant across all cells. We determine the cell energy by using the average energy value of all possible transitions for the n-bit cell. The TiO$_2$ cell energy dominates the energy dissipated in all the array components due to large set/reset time and lower resistance values for TiO$_2$ RRAM, while the HfO$_x$ cell energy is much smaller than the energy in the remaining array components. The minimum total write energy/operation is consumed at n=3 for both cases.

### 3.7 Memory Technology Comparison

In this section, we compare the performance and energy of the designed multi-bit array with other types of memory technologies. Figures 3·18 and 3·19 show a comparison of the
read and write time vs. energy of different state-of-the-art memory technologies with the designed multi-bit $TiO_2$/$HfO_x$-based RRAM array. For $TiO_2$ and $HfO_x$ we consider the minimum energy points corresponding to different number of bits/cell in uniform state assignment scheme. The optimized multi-bit RRAM array designed in this work has lower energy consumption compared to other emerging nonvolatile memory technologies such as MRAM, FeRAM and PCRAM based on recently-published measurement data. The write access time of $HfO_x$ RRAM is small compared to other types of nonvolatile memory technologies but the $TiO_2$ RRAM write time is large. On the other hand, the read access time of $HfO_x$ RRAM is large compared to other types of nonvolatile memory technologies but the $TiO_2$ RRAM read time is small. The lower energy and access time of the optimized multi-bit RRAM array makes it a promising replacement for CMOS-based nonvolatile memory technologies.

3.8 PVT Variation Analysis of n-bit RRAM Cell

As was mentioned in section 2.1, OTF and LER cause variations in memristor geometry (Niu et al., 2010b), (Hu et al., 2011b), (Hu et al., 2011a) and RDD causes randomness in resistivity which directly impacts the performance and energy dissipation of RRAM cells. In this section, we apply the Monte-Carlo methodology (Hu et al., 2011a) to our models for
both TiO$_2$-based and HfO$_x$-based memristors to analyze the influence of OTF, LER and RDD on the performance and energy of the n-bit 1T1R RRAM cell. For our analysis, we exclude the variations in the energy and performance of the CMOS devices due to PVT variations to isolate and quantify the true impact of PVT variations on the memristors device functionality and the cell as a whole.

The LER of the memristor has been modeled as a combination of the low and high frequency domain disturbances in (Hu et al., 2011a), and (Wang et al., 2009), and is given by

$$LER = L_{LF} \sin(f_{\text{max}}.r) + L_{HF}.z$$  \hspace{1cm} (3.12)$$

where the sinusoid function with the amplitude of $L_{LF}$ describes the low frequency domain variations. Here $f_{\text{max}} = 1.8 \text{ MHz}$ is the mean of the low frequency range with a uniform distribution represented as $r \in U(-1,1)$. $L_{HF}$ accounts for the high frequency variations and $z$ is considered to have a normal distribution function as $N(0,1)$. The effect of OTF is usually modeled as a Gaussian distribution with a $\sigma = 2\%$ deviation from the nominal
memristor thickness (Hu et al., 2011a), (Niu et al., 2010b). Also RDD has been modeled as having a Gaussian distribution with $\sigma = 2\%$ (Hu et al., 2011b) in the resistivity term in both ionic drift and filament growth models for TiO$_2$ and HfO$_x$-based RRAMs.

Considering the nominal parameters in Table 2.1, we explore the effect of OTF, LER, and RDD on the states of both TiO$_2$-based and HfO$_x$-based RRAMs. The state definition for ionic drift-based TiO$_2$ RRAM model is only a function of the ratio of the doped region to memristor thickness. The movement of dopants along the memristor thickness defines memristance (see Figure 2·1a). Therefore, the state assignment will only be affected by OTF. In other words, LER and RDD will not change the state assignment of TiO$_2$-based RRAMs according to ionic drift memristor model. The impact of OTF on TiO$_2$-based RRAM with uniform and non-uniform state assignments for different number of stored bits ($1 \leq n \leq 4$) for 10000 samples are illustrated in Figures 3·20 and 3·21. The multi-bit TiO$_2$-based 1T1R RRAM cell is resilient to OTF-based process variations up to n=3 for uniform state assignment and up to n=2 for non-uniform state assignment, where no overlap is observed between adjacent states.
The state definition for filament growth-based $HfO_x$ RRAM model is only a function of filament diameter. Therefore, the state assignment will only be affected by LER. OTF and RDD will not change the state assignment of $HfO_x$-based RRAMs. The uniform and non-uniform state distributions of the $HfO_x$-based RRAM for different number of stored bits ($1 \leq n \leq 4$) are illustrated in Figure 3.22 and 3.23. The multi-bit $HfO_x$-based 1T1R RRAM cell is resilient to LER-based process variations up to $n=3$ where no overlap is observed between adjacent states.

Table 3.4 summarizes the effect of LER, OTF and RDD on the state assignment, write time, write energy, read energy and read destructiveness of the 3-bit $TiO_2$-based and $HfO_x$-based 1T1R cells. As discussed earlier, the $TiO_2$ memristor state is only affected by OTF whereas the $HfO_x$ memristor state is only affected by LER. The impact of LER, OTF and RDD is quantified as $(3\sigma/\mu) \times 100\%$ value of each parameter. OTF has higher impact on the $TiO_2$ specifications compared to LER. Also OTF has the highest impact on the write time variations for the multi-bit $TiO_2$ memristor since the $TiO_2$ set/reset time is a quadratic function of memristor thickness based on (3.5). Similarly, the effect of OTF on the write energy and read destructiveness of the $TiO_2$ RRAM is higher than LER. The variation in read destructiveness changes the refresh threshold which affects the reliability of read operation. OTF and LER have similar impact on read energy since it is mostly dominated by bitline variations according to (3.8). It should be noted that OTF has a minimal impact on the write time and read destructiveness of the $HfO_x$-based 1T1R cell as these two parameters are independent of the oxide thickness (see equations (2.7) and (3.6)). LER has the highest impact on the write energy variations of the multi-bit $HfO_x$ memristor due to its sensitivity to filament diameter fluctuations based on (3.11). The rate of change of diameter in the filament growth model has higher sensitivity to RDD at lower voltages. In other words, high set/reset voltages limit the effect of RDD in write time variations of $HfO_x$-based RRAMs. However, read destructiveness significantly changes with RDD since the applied read voltages are considerably low compared to write (set/reset) voltages which deteriorates the read reliability of the $HfO_x$-based RRAMs.

The power supply noise in VLSI chips causes variations in the supply voltage applied to the various transistors in a circuit, which in turn causes variations in performance and energy dissipation. Table 3.5 summarizes the impact of voltage variations on write time,
write energy, read energy and read destructiveness of a 3-bit RRAM cell. Without loss of
generality, we explore two cases where each voltage reference has been assumed to have a
Gaussian distribution with $3\sigma = 6\%$ and $3\sigma = 10\%$ of the nominal value. We calculate the
write time and energy variations considering 56 possible transitions for the 3-bit 1T1R RRAM
cell. The write time and write energy of the $HfO_x$ RRAM has more variations compared to
$TiO_2$ since these two parameters are exponential functions of applied voltage in $HfO_x$ RRAM
according to (3.6) and (3.11). Comparing the rate of state change in equations (2.2) and
(2.7), the destructiveness of the $HfO_x$-based memristor state is considerably more sensitive
to voltage fluctuations. This will significantly affect the refresh threshold in Equation (3.3)
(see Table 3.5). The read energy has similar amount of variations due to voltage fluctuations.
for both materials according to (3.8).

We also analyzed the impact of temperature variations on performance and energy metrics of both TiO$_2$-based and HfO$_x$-based memristors in the 3-bit RRAM cell. The temperature dependency of the ionic drift model has been modeled in (Strukov and Williams, 2011) where thermal resistance of the filament, defined as the ratio between the maximum temperature increase in the filament and the dissipated electrical power (Russo et al., 2009), for the state 1 ($R_{ON}$) and state 0 ($R_{OFF}$) in the TiO$_2$ filament are derived as:

\[
R_{th}(R_{ON}) = \frac{L}{(8k_M A_{CF})} \tag{3.13}
\]

\[
R_{th}(R_{OFF}) \approx \left(2\text{ArcSinh}[L/\sqrt{A_{CF}}] - 1.5\right)/(4k_I L). \tag{3.14}
\]

Here, \( k_M = 30W/mK \) and \( k_I = 3W/mK \) (Strukov and Williams, 2011) are the thermal conductances of the metal and insulator corresponding to titanium oxide thin films with oxygen vacancies conductive channels and \( A_{CF} \) is the filament area. The change in resistance of the RRAM based on ionic drift model follows \( \Delta R_{R_{OFF},R_{ON}} \propto \Delta T/(R_{th}I^2) \) where \( I \) is the RRAM current.

Table 3.6 summarizes the impact of temperature variations on write time, write energy, read energy and destructiveness of both TiO$_2$-based and HfO$_x$-based memristors in the 3-bit RRAM cell. We explore two cases with nominal ambient temperature and variations of \( \Delta T = 10K \) and \( \Delta T = 30K \). Temperature variations have a larger impact on the read destructiveness of the HfO$_x$-based memristor. The rate of change of diameter in HfO$_x$-based RRAMs due to temperature variations increases at lower applied voltages based on filament growth model in (2.4) (see Figure 3·24). The variations in write time and write energy of HfO$_x$ RRAM is higher than TiO$_2$ due to the exponential temperature term in these metrics for HfO$_x$ RRAM. The effect of temperature variation on the intermediate states of the multi-bit TiO$_2$ RRAM can be analyzed using the effective thermal resistance as \( R_{th} = R_{th}(R_{ON})||R_{th}(R_{OFF}) \) (Strukov and Williams, 2011) where the corresponding cross-section area for each state is plugged into the two thermal resistance expressions in (3.13) and (3.14). The effective thermal resistance of a 3-bit TiO$_2$-based RRAM is illustrated in Figure 3·25 for different memristor states. Temperature variations have minimal effect on the read
energy fluctuations of $TiO_2$ RRAM since it is mostly affected by bitline resistance (according to (3.8)). This is however not the case for the $HfO_x$ RRAM since its typical $R_{OFF}$ value is orders of magnitude larger than the bitline resistance according to Table 2.1. This will dominate the effect of temperature variations in $HfO_x$ RRAM read energy fluctuations with respect to bitline parasitic variations.

### 3.9 Summary

In this chapter, we presented the design and optimization of a n-bit 1T1R RRAM array designed using $TiO_2$- and $HfO_x$-based memristors. We first presented models for performance and energy of read and write operation in n-bit 1T1R RRAM cells designed using $TiO_2$- and $HfO_x$-based memristors. We validated our performance and energy models against HSPICE simulations, and the difference is less than 10% for both n-bit $TiO_2$- and $HfO_x$-based 1T1R cells. Using energy and performance constraints, we determined the optimum number of bits/cell in the multi-bit RRAM array to be 3. The total write and read energy of the 3 bits/cell $TiO_2$-based RRAM array was 4.06 pJ/bit and 188 fJ/bit for 100 nsec and 1 nsec write and read access times while the optimized 3 bits/cell $HfO_x$-based RRAM array consumed 365 fJ/bit and 173 fJ/bit for 1 nsec and 200 nsec write and read access times, respectively. We explored the trade-off between the read energy consumption and the robustness against process variations for uniform and non-uniform memristor state assignments in the multi-bit RRAM array. Using the proposed models, we analyzed the effects of process, voltage and temperature variations on performance and energy consumption and the reliability of n-bit 1T1R memory cells. Our analysis showed that multi-bit $TiO_2$ RRAM is more sensitive to OTF while $HfO_x$ RRAM is more sensitive to LER and is more susceptible to voltage and temperature variations.
Chapter 4

Sub-threshold Logic Design using Feedback Equalization

4.1 Introduction

In addition to using memristors as storage elements, we are exploring the use of memristors in logic circuits. In particular, we are investigating the use of memristors in the design of feedback equalizer circuits for digital logic circuits. The key idea here is to explore the use of communications-inspired techniques in the design of robust energy-efficient digital logic circuits. Feedback equalization for above-threshold regime has previously been proposed by (Takhirov et al., 2012) and we will explore it for sub-threshold circuits. Using a feedback equalizer circuit that adjusts the switching thresholds of the gates (just before the flip flops) based on the prior sampled outputs, we can reduce the propagation delay of the critical path in the combinational logic block to make the sub-threshold system more robust to timing errors and at the same time reduce the dominant leakage energy of the entire design.

4.2 Related Work

Several circuit topologies operating in sub-threshold regime have been proposed in the literature for ultra low-power applications. In (De Vita and Iannaccone, 2007) the authors have used a current reference circuit to design a voltage regulator providing a supply voltage that makes the propagation delay of the sub-threshold digital circuits almost insensitive to temperature and process variations. Using differential dynamic logic in standby mode, the authors in (Liu and Rabaey, 2012) managed to significantly suppress leakage in an adaptive neural signal processor. A latch-based sub-threshold FPGA using low-power basic logic elements (BLE) has been presented in (Grossmann et al., 2012). Proposing an ultra low-power clock circuit to the digital logic, the authors in (Mishra et al., 2013) have discussed the design of a management circuit implemented in 0.18 μm CMOS technology that provides a nanowatt power management scheme suitable for wireless sensor network applications where batteries are not practical. Using a configurable ring oscillator that compensates the delay variation of the critical path, the authors in (Luetkemeier et al., 2012) have reported the measurement results of a 32-bit sub-threshold processor with adaptive supply voltage control. The minimum energy point of the fabricated design is at 325 mV.

A detailed analysis on the timing variability and the metastability of the flip flops de-
signed in sub-threshold region has been proposed in (Lotze et al., 2008) and (Li et al., 2011), respectively. Using near-threshold friendly flip flops, multiplexers and level converters, the authors in (Kaul et al., 2012) have analyzed the required techniques for reliable operation of weak inversion logic circuits. A custom sub-threshold cell library has been proposed in (Kwong et al., 2009) to address output voltage failures and propagation delays in logic gates. The authors in (Zhou et al., 2011) managed to boost the drain current of the transistors using minimum-sized devices with fingers to mitigate the inverse narrow width effect in sub-threshold domain. An analytical framework for sub-threshold logic gate sizing based on statistical variations has been proposed in (Liu et al., 2012) which provides narrower delay distributions compared to the state-of-the-art approaches in 90 nm CMOS technology node. The authors in (Lotze et al., 2010) proposed a timing model that characterizes the actual transistor-level waveforms in sub-threshold voltages with 3% average error. The temperature dependence of the within-die random gate delay variations in sub-threshold logic circuits is modeled in (Takahashi et al., 2012).

The authors in (Takhirov et al., 2012) developed a circuit-level technique which uses the Feedback Equalization with Schmitt Trigger (FEST) to suppress the intersymbol interference (ISI) resulting from aggressive voltage scaling in CMOS digital circuits. Using the FEST circuit, they lower down the critical supply voltage of a 4-bit Kogge-Stone adder as well as a 3-tap 4-bit finite impulse response (FIR) filter leading to 20% and 40% decrease in the total consumed energy, respectively. The authors in (Takhirov et al., 2013) proposed an equalized pass-transistor logic (E-PTL) design technique which consumes between 15% to 30% lower energy per operation than PTL and static CMOS logic, respectively.

We propose a circuit-level scheme that uses a communications-inspired feedback equalization technique in the critical path to mitigate the timing errors rising from aggressive voltage scaling in sub-threshold digital logic circuits. It should be noted that we are not designing sub-threshold communication circuits. We are proposing the design of sub-threshold logic circuits that leverage principles of communication theory. Using feedback equalizer circuits, we further scale down the operating voltage of the sub-threshold circuit at the minimum energy supply voltage to decrease the dynamic power as well as the leakage power in sub-threshold CMOS circuits. We also propose to increase the operating frequency of the sub-threshold circuits at the fixed supply voltage to reduce the leakage energy.

4.3 Equalized Flip flop versus Conventional Flip flop

In this section, we first explain the use of the feedback equalizer circuit in the design of an equalized flip flop and then provide a detailed comparison of the equalized flip flop with a conventional flip flop in terms of area, setup time and performance. We propose the application of a feedback equalizer (designed using a variable threshold inverter (Sridhara et al., 2008) shown in Figure 4-1) along with the classic master-slave positive edge-triggered flip flop (Rabaey et al., 2003) to implement an equalized flip flop. The equalized flip flop dynamically modifies the switching threshold of the gate before the flip flop based on the previous sampled data. If the previous output of the gate is a zero, the equalized flip flop lowers
Figure 4.1: Feedback equalizer (designed using a variable threshold inverter (Sridhara et al., 2008)) can be combined with a traditional master-slave flip flop to design an equalized flip flop.

down the switching threshold which speeds up the transition to one. Similarly if the previous output is one, the equalized flip flop increases the switching threshold which speeds up the transition to zero. In this configuration, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions. The DC response of the feedback equalizer circuit in sub-threshold regime is shown in Figure 4.2. The switching of the variable threshold inverter is dynamically adjusted based on the previous sampled output data. Compared to the above-threshold regime, the reduced noise margin in weak inversion region does not allow for aggressively overscaling the supply voltage while using the variable threshold inverter. So we do not use the Schmidt Trigger circuit along with the feedback equalizer circuit as proposed in (Takhirov et al., 2012) for above-threshold operation. The equalized flip flop has 6 transistors more than the conventional master-slave positive edge-triggered flip flop (Rabaey et al., 2003). Compared to a classic master-slave flip flop with 22 transistors (7 inverters and 4 transmission gates (TG)), the area overhead of the equalized flip flop is around 27%. This area overhead gets amortized across the critical path of the sub-threshold logic.

The total power consumed by a digital circuit can be calculated using

\[ P_T = P_{DY} + P_L = C_{eff} V_{DD}^2 f + I_{leak} V_{DD} \]

In Equation (4.1), \( P_{DY} \) and \( P_L \) are the dynamic and leakage power components of the digital circuit, respectively. \( C_{eff} \) is the average total capacitance of the entire circuit, \( V_{DD} \) is the supply voltage and \( f \) is the operating frequency of the circuit. \( I_{leak} \) is the leakage current and can be written as

\[ I_{leak} = \mu_0 C_{ox} \frac{W}{L} (n-1) V_{th}^2 n^{\eta} \frac{V_{dd} - V_T}{n V_{th}} \]

In Equation (4.2), \( V_T \) is the transistor threshold voltage, \( V_{th} \) is the thermal voltage, \( n \) is the sub-threshold slope factor and \( \eta \) is the DIBL coefficient. There is an exponential relationship between the leakage current and the supply voltage (due to the DIBL effect

37
Table 4.1: Comparison between the characteristics of the equalized flip flop (E-flip flop) with the conventional non-equalized master-slave flip flop (NE-flip flop) at different supply voltages operating in sub-threshold regime. Feedback equalization technique reduces the propagation delay of the 8-bit carry-lookahead adder CMOS logic whereas the setup time and \( t_{c-q} \) delay of the conventional flip flop is smaller than the equalized flip flop.

<table>
<thead>
<tr>
<th>Supply voltage (mV)</th>
<th>Delay E-logic (nsec)</th>
<th>Delay NE-logic (nsec)</th>
<th>( t_{c-q} ) E-flip flop (nsec)</th>
<th>( t_{c-q} ) NE-flip flop (nsec)</th>
<th>Setup time E-flip flop (nsec)</th>
<th>Setup time NE-flip flop (nsec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>350</td>
<td>226</td>
<td>255</td>
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<td>3.82</td>
<td>8.62</td>
<td>6.07</td>
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<tr>
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<td>5.66</td>
<td>12.80</td>
<td>9.01</td>
</tr>
<tr>
<td>310</td>
<td>489</td>
<td>532</td>
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<td>13.11</td>
</tr>
<tr>
<td>290</td>
<td>750</td>
<td>842</td>
<td>12.72</td>
<td>12.61</td>
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</tr>
<tr>
<td>270</td>
<td>1064</td>
<td>1159</td>
<td>18.04</td>
<td>17.87</td>
<td>40.49</td>
<td>28.49</td>
</tr>
<tr>
<td>250</td>
<td>1661</td>
<td>1820</td>
<td>28.15</td>
<td>27.89</td>
<td>63.20</td>
<td>44.46</td>
</tr>
</tbody>
</table>

and for \( V_{DS} \approx V_{DD} \). Using the equalized flip flop, we can scale down the supply voltage while maintaining the zero word error rate at a given operating frequency and achieve lower dynamic power consumption (due to the quadratic relationship between the dynamic power and the supply voltage) as well as lower leakage power (due to smaller DIBL effect which exponentially decreases the leakage current). Similar to the area overhead, the dynamic power as well as the leakage overhead of the variable threshold inverter gets amortized across the entire sub-threshold combinational logic block.

Figure 4.3 illustrates the timing waveforms of the output carry bit of an 8-bit carry-lookahead adder implemented in UMC 130 nm process using static complementary CMOS logic. In the figure, we show the waveform for the input node of the non-equalized flip flop (NE-flip flop), the input node of the equalized flip flop (E-flip flop), the latched output for both cases and the output node of the variable threshold inverter. Compared to the signal at the input node of the non-equalized flip flop, the variable threshold circuit provides sharper transitions and decreases the propagation delay of the critical path of the sub-threshold logic. However, it should be noted that excessive positive feedback might lead to increased glitches at the input of the equalizer which increases the probability of occurrence of timing errors. Therefore, the transistors in variable threshold inverter need to be carefully sized to avoid the errors rising due to the glitches.

It has been shown in (Rabaey et al., 2003) that the setup time of the conventional master-slave positive edge-triggered flip flop is \( t_{setup} = 3t_{inv} + t_{TG} \). Since the equalized flip flop uses an extra variable-threshold inverter at its output, the setup time of the equalized flip flop will be larger \( t_{setup} \approx 4t_{inv} + t_{TG} \). The \( t_{c-q} \) delay of the conventional flip flop is \( t_{c-q} = t_{inv} + t_{TG} \). Since the equalized flip flop has the variable threshold inverter as extra load at the output, the \( t_{c-q} \) delay of the equalized flip flop is \( t_{c-q} = t_{inv} + \Delta t + t_{TG} \) which is slightly larger than the \( t_{c-q} \) delay of the conventional flip flop. Here \( \Delta t \) is the increase in inverter delay due to the extra load. However, the feedback equalizer circuit can significantly lower down the propagation delay of the critical path by providing a faster charging (or discharging) path for
Figure 4.2: DC response of the variable threshold circuit in sub-threshold regime. The switching threshold of the inverter is modified based on the previous sampled output data.

Figure 4.3: Comparison between the timing waveforms of the input node of the conventional flip flop (A), output node of the conventional flip flop (B), input node of the equalized flip flop (C), output node of the equalized flip flop (D), output node of the variable threshold inverter (E). Feedback circuit makes sharper transitions in the waveforms of the logic output node helping the equalized flip flop sample the correct data.

The input capacitance of the flip flop. Table 4.1 compares the propagation delay, setup time and the $t_{c-q}$ delay of the two 8-bit carry-lookahead adders designed with conventional flip flop and equalized flip flop in UMC 130 nm when operating with different supply voltages. The variable threshold inverter has been accurately sized to minimize the total delay of the critical path.
Figure 4.4: Operating frequency of the 8-bit carry lookahead adder for zero word error rate as function of different sub-threshold supply voltages. The equalized logic (E-logic) can run 22.87% (on average) faster than the non-equalized logic (NE-logic).

Figure 4.5: Comparison between the total consumed energy as well as the dynamic/leakage components of the 8-bit carry lookahead adder for different supply voltages. At the minimum energy supply voltage, the equalized logic is burning 18.4% less total energy compared to the non-equalized version.

4.4 Experimental Results

In this section, we perform a detailed comparison, in terms of performance and energy consumption, of a sample 8-bit carry-lookahead adder designed in UMC 130 nm process using both equalized and non-equalized flip flops. We analyze the impact of the proposed feedback equalization technique when the frequency of the sub-threshold logic is improved at a fixed supply voltage and also when the energy of the sub-threshold logic is reduced by scaling down the supply voltage at a fixed operating frequency. We also explore the use of the proposed feedback equalizer circuit to reduce the amount of transistor oversizing for mitigating the process variation effects.

4.4.1 Performance improvement at the fixed supply voltage

We first explore the case where the feedback equalizer circuit reduces the rise/fall time of the last gate and hence the critical path of the combinational logic block leading to a higher operating frequency. The variable threshold inverter can be used to reduce the propagation
delay of the critical path at any operating supply voltage. Figure 4-4 shows the operating frequency of the 8-bit carry lookahead adder for different sub-threshold supply voltages at zero word error rate when using an equalized and conventional flip flop. Here, we determined the optimum sizing for the feedback equalizer circuit that minimizes the propagation delay of the critical path and prevents glitches for zero error rate operation at each supply voltage data point. The sizing of the combinational logic block is the same for both the equalized and non-equalized circuit and is determined using the design methodology described in (Kwong et al., 2009) to address the degraded noise margin levels in sub-threshold regime. The operating frequency of the equalized logic is 22.87% (on average) higher than the non-equalized logic over the range of 250 mV to 350 mV. The amount of performance acceleration in aggressively scaled supply voltages is more promising compared to voltages close to the threshold as the variable threshold inverter is capable of significantly decreasing the large transition times of the logic designed in deep sub-threshold region. At 250 mV supply voltage, the equalized flip flop improves the operating frequency of the logic by 27.8% whereas the amount of performance improvement at 350 mV is 16.2%.

By reducing the propagation delay of the critical path, the feedback equalizer circuit is capable of reducing the dominant leakage energy of the digital logic in sub-threshold regime. Figure 4-5 illustrates a head-to-head comparison between the total energy, the dynamic energy and the leakage energy of the 8-bit carry lookahead adder for different supply voltages while using the equalized or conventional non-equalized flip flops. By adding the feedback equalizer to the conventional flip flop, the dynamic energy of the logic with the equalized flip flop is 3.47% (on average) larger than the logic designed with non-equalized conventional flip flop. This is negligible compared to the 22.6% reduction in the leakage component of the design. At the minimum energy supply voltage, the equalized logic consumes 18.4% less total energy compared to the non-equalized version. The feedback circuit drops the minimum energy supply voltage of the logic by 10 mV while maintaining the zero word error rate operation.

The leakage energy reduction mechanism of the feedback equalization technique in sub-threshold regime is due to the fact that the total delay along the critical path of the equalized logic decreases (the sub-threshold CMOS logic is running faster) leading to lower leakage energy according to (Kwong et al., 2009)

\[ E_T = E_{DY,N} + E_L = C_{eff}V_{DD}^2 + I_{leak}V_{DD}T_D \] (4.3)

In Equation (4.3), \( E_T \) is the total dissipated energy, \( E_{DY,N} \) and \( E_L \) are the dynamic and leakage components, respectively. \( T_D = 1/f \) is the total delay along the critical path of a digital circuit.

Decreasing the dominant leakage energy component of the sub-threshold logic together with reducing the propagation delay of the critical path, the feedback equalization technique lowers the energy-delay product of the logic designed in weak inversion region. On average, the equalized 8-bit carry lookahead adder has 30.44% smaller energy-delay product value compared to the non-equalized logic over the range of 250 mV to 350 mV for zero word error rate operation. If we compare the energy-delay product at the respective minimum
Table 4.2: Comparison between the minimum energy point and the corresponding operating frequency of the equalized logic (E-logic) vs. non-equalized (NE-logic) design of various logic blocks.

<table>
<thead>
<tr>
<th>Logic block</th>
<th>NE-logic Energy (fJ/cycle)</th>
<th>E-logic Energy (fJ/cycle)</th>
<th>NE-logic Frequency (MHz)</th>
<th>E-logic Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-bit CLA</td>
<td>12.63</td>
<td>10.3</td>
<td>1.28</td>
<td>1.62</td>
</tr>
<tr>
<td>8-bit Multiplier</td>
<td>16.27</td>
<td>15.24</td>
<td>1.22</td>
<td>1.49</td>
</tr>
<tr>
<td>8-bit FIR filter</td>
<td>100.32</td>
<td>94.84</td>
<td>0.64</td>
<td>0.71</td>
</tr>
</tbody>
</table>

Figure 4-6: Comparison between the energy consumed by the equalized (E-logic) vs. non-equalized (NE-logic) 8-bit carry lookahead adder for different supply voltages with fixed performance ($f = 1.28 \text{ MHz}$) at zero word error rate. The non-equalized logic design consumes minimum energy at 300 mV. The equalized flip flop enables 30 mV supply voltage scaling leading to 16.72% lower total consumed energy. The equalized flip flop cannot operate at $V_{DD} < 270\text{mV}$ due to the occurrence of timing errors.

energy supply voltages, the equalized flip flop reduces the energy-delay product of the 8-bit carry lookahead adder by 35.4%. Table 4.2 compares the minimum energy point and the corresponding operating frequency of the equalized logic design (E-logic) vs. non-equalized logic design (NE-logic) of an 8-bit carry lookahead adder (CLA), 8-bit Array Multiplier and 3-tap 8-bit FIR filter, all designed in UMC 130 nm process. On an average, the equalization technique has 24.49% lower energy-delay product than the non-equalized logic design.

4.4.2 Leakage reduction at the fixed operating frequency

As described in Section 4.3, the equalized flip flop can be used to scale supply voltages (while maintaining the operating frequency) to lower down the dominant leakage energy by decreasing the leakage current of the sub-threshold logic. We designed the feedback equalizer circuit for each scaled supply voltage that ensured the reliable operation of the equalized design without any timing errors. Figure 4-6 illustrates the dynamic and leakage energy components of the 8-bit carry lookahead adder at the minimum energy supply voltage (of
the non-equalized design) and below. The operating frequency of all design points with zero word error rate is $f = 1.28 \, MHz$ (the frequency of the minimum energy supply voltage for the non-equalized design). Compared to the non-equalized design, the equalized design can operate at 30 $mV$ lower supply voltage leading to 16.72% lower energy consumption. The equalized design cannot operate for $V_{DD} < 270 \, mV$ due to the larger rise/fall times that lead to timing errors.

4.4.3 Mitigating process variations

Using the proposed feedback-based technique, the critical sizing approach used for designing the sub-threshold logic circuits in (Kwong et al., 2009) can be relaxed. The transistor sizing can be scaled down while ensuring the reliable operation using feedback equalizer circuit in presence of process variations. For the 8-bit carry-lookahead adder in UMC 130 $nm$ process, the transistors sized using (Kwong et al., 2009) ($W_{baseline}$) can be scaled down to 75% × $W_{baseline}$ while matching the operating frequency of the equalized design and non-equalized design. Figure 4.7 illustrates the energy-delay product of the scaled down equalized logic and baseline non-equalized logic for different sub-threshold supply voltages. At a given voltage, compared to the non-equalized design, the equalized design uses smaller transistors and has lower propagation delay resulting in a reduction of both dynamic and leakage energy. For a $3\sigma_{V_T} = 30 \, mV$ variation in threshold voltage, the equalized design can reliably operate without the occurrence of any timing errors. Table 4.3 summarizes the amount of energy savings of the equalized logic with scaled down transistors compared to the baseline non-equalized and the equalized logic where the combinational logic has been sized according to the method proposed in (Kwong et al., 2009). Overall the feedback equalization along with transistor size scaling consumes up to 20.72% lower total energy compared to the conventional non-equalized design in sub-threshold regime.
Table 4.3: Energy savings in scaled-down equalized logic compared to baseline non-equalized and equalized logic at the minimum energy supply voltage at zero word error rate operation for 8-bit carry lookahead adder.

<table>
<thead>
<tr>
<th>Scaled-down equalized logic size</th>
<th>Total energy saving w.r.t non-equalized</th>
<th>Total energy saving w.r.t equalized</th>
</tr>
</thead>
<tbody>
<tr>
<td>95%×W_{baseline}</td>
<td>12.87%</td>
<td>6.72%</td>
</tr>
<tr>
<td>85%×W_{baseline}</td>
<td>16.79%</td>
<td>10.92%</td>
</tr>
<tr>
<td>75%×W_{baseline}</td>
<td>20.72%</td>
<td>15.12%</td>
</tr>
</tbody>
</table>

Figure 4.8: Energy-delay product of a 8-bit carry lookahead adder designed using equalized logic (E-logic) vs. non-equalized logic (NE-logic) at zero word error rate at different technology nodes. The equalized logic approach reduces the energy-delay product of the sub-threshold logic by up to 26.46% across all technology nodes in the minimum energy supply voltage.

4.5 Effect of Technology Scaling

In this section, we analyze the effect of technology scaling on the performance improvement and the energy reduction obtained using feedback equalization technique in sub-threshold regime. In scaled technology nodes, the contribution of leakage energy component dominates due to larger DIBL effect as well as smaller $V_T$ values. Running the sub-threshold logic faster, the equalizer will more effectively reduce the leakage energy component and in turn decrease the energy-delay product in scaled technology nodes. Figure 4.8 illustrates the value of the energy-delay product of the 8-bit carry lookahead adder designed using PTM (Ptm, ) for 4 different technology nodes and operating at zero word error rate at minimum energy supply voltage. Compared to the non-equalized logic design, the energy-delay product of the equalized logic design is 20.45%, 24.32%, 27.82% and 33.25% smaller at 130 nm, 90 nm, 65 nm and 45 nm technology nodes, respectively. On average, the equalized flip flop reduces the energy-delay product of the sub-threshold logic by up to 26.46% across all technology nodes at the minimum energy supply voltage.
4.6 Summary

In this chapter, we proposed the application of a variable threshold inverter-based feedback equalization circuit to reduce the dominant leakage energy of the digital CMOS logic operating in sub-threshold regime. Adjusting the switching thresholds based on the prior sampled outputs, the feedback equalization circuit enables a faster switching of the logic gate outputs and provides the opportunity to reduce the leakage current in weak inversion region. We implemented a non-equalized and an equalized design of an 8-bit carry lookahead adder in UMC 130 nm process using static complementary CMOS logic and managed to reduce the propagation delay of the critical path of the sub-threshold logic and correspondingly lower the dominant leakage energy, leading to 35.4% decrease in energy-delay product of the conventional non-equalized design at minimum energy supply voltage. Using the feedback equalizer circuit, we obtained 16.72% reduction in energy through voltage scaling while maintaining an operating frequency of 1.28 MHz. We showed that the equalized sub-threshold 8-bit carry lookahead adder requires lower upsizing to tolerate process variation effects leading to 20.72% lower total energy.
Chapter 5

Future Work

In Chapter 3, we described the design and optimization of nonvolatile multi-bit RRAM arrays using $\text{TiO}_2$ and $\text{HfO}_x$ memristor technologies, and in Chapter 4, we described the feedback equalization technique to reduce the leakage energy of the digital logic circuits designed in sub-threshold regime. Moving forward, we plan to explore the use of the memristor technology to develop an adaptive feedback equalization technique for digital logic design. In this chapter, we provide a brief overview of the research topics that we will pursue.

Chapter 4 shows the benefits of feedback equalization technique in reducing the dominant leakage energy component of digital logic circuits designed in sub-threshold regime. We will explore the application of a memristor-based feedback equalization technique for adaptive tunable logic circuit design. The use of a memristor-based feedback topology decreases the area/leakage overhead of the equalized flip flop and provides the opportunity to dynamically adjust the feedback strengths and tune the digital logic block with respect to performance, energy and error rate constraints. This tunability of the feedback strength is possible by tuning the memristance value of the memristor in the feedback topology. We will also develop the required peripheral circuitry for programming the equalizer circuit and determine its corresponding overhead. The following activities will be completed as part of the future work:

- Design and optimize a CMOS-based adaptive equalizer circuit topology having various feedback strengths to dynamically tune the designed digital logic and meet the required performance constraints for a energy and error rate budget. (4 month)

- Develop memristor-based feedback equalizer circuit as a replacement to the CMOS-based feedback equalizer circuits. (2 months)

- Model the performance, energy and error rate of the proposed memristor-based feedback equalizer circuit. (2 months)

- Analyze the destructiveness of the proposed memristor-based feedback equalizer circuit for different feedback strengths. (1 months)

- Design the peripheral circuitry used to tune the memristor and calculate the delay, energy and area overhead of the peripheral circuitry used to program the RRAM device component of the feedback equalizer circuit for different feedback strengths. (2 months)
<table>
<thead>
<tr>
<th>Task Name</th>
<th>Q4</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
</tr>
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<tbody>
<tr>
<td>Design a CMOS-based adaptive equalizer circuit topology having various feedback strengths to dynamically tune the designed digital logic</td>
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<tr>
<td>Develop memristor-based feedback equalizer circuit as a replacement to the CMOS-based feedback equalizer circuits</td>
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<tr>
<td>Model the performance, energy and error rate of the proposed memristor-based feedback equalizer circuit</td>
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<td>Analyze the destructiveness of the proposed memristor-based feedback equalizer circuit for different feedback strengths</td>
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<tr>
<td>Design the peripheral circuitry used to tune the memristor and calculate the delay, energy and area overhead of the peripheral circuitry used to program the RRAM device component of the feedback equalizer circuit for different feedback strengths</td>
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<tr>
<td>Compare the memristor-based feedback equalizer circuit with the conventional CMOS-based feedback equalizer circuit in terms of power, performance and area</td>
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Figure 5.1: Gantt chart showing the timeline of the post-prospectus plans.

- Compare the memristor-based feedback equalizer circuit with the conventional CMOS-based feedback equalizer circuit in terms of power, performance and area. (1 months)
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