

TABLE I
FAULT CLASSES USED FOR THE TWO-STAGE
FOUR-OP-AMP BIQUAD CIRCUIT. THE NOMINAL AND FAULTY
VALUES ARE ALSO SPECIFIED

Fault Class	Nominal	Faulty Value
C1 ↑	0.01 μ F	0.051 μ F
C2 ↑	0.01 μ F	0.02 μ F
C3 ↑	0.01 μ F	0.048 μ F
C4 ↑	0.01 μ F	0.031 μ F
R16 ↑	1800 Ω	7800 Ω
R17 ↓	4840 Ω	1600 Ω
R19 ↑	10000 Ω	30000 Ω
R21 ↓	10000 Ω	3750 Ω
R22 ↑	2320 Ω	7000 Ω
R3 ↓	2200 Ω	5000 Ω
R4 ↓	1570 Ω	600 Ω
R6 ↑	10000 Ω	16500 Ω
R7 ↓	10000 Ω	5500 Ω
R8 ↑	440 Ω	2200 Ω
R9 ↑	2640 Ω	4300 Ω

these three faults must be placed in the same ambiguity group if the circuit output is the only measure to determine fault classes. Training the neural network on more than one node voltage or using testability analysis as a preprocessor [12] can further resolve the ambiguity groups. For instance, if the training data for the lowpass filter includes features associated with the v_2 node voltage, our neural network can classify $R9 \uparrow$ fault correctly and the ambiguity group reduces to $R6 \uparrow$ and $R7 \downarrow$. Our results clearly indicate that through appropriate preprocessing of an analog circuit output, one can train a neural network to correctly diagnose all faults unless the circuit's outputs are similar for some fault classes.

VI. CONCLUSION

We have applied backpropagation neural networks with wavelet decomposition, PCA, and data normalization as preprocessors to fault diagnosis of analog circuits. Our study indicates that the proposed preprocessing techniques have a significant impact on analog fault diagnosis due to the selection of an optimal number of relevant features. This leads to neural network architectures with minimal size that can be trained efficiently and carry out fault diagnosis with a high degree of accuracy. For complex analog circuits, our approach leads to neural networks that can identify individual faulty components unless these faults give similar circuit outputs. In such a case, the neural network can identify the ambiguity group containing the fault classes with similar outputs. Further resolution of ambiguity groups is possible by addition of features from more node voltages to train the neural network. Since our analog fault-diagnostic system is based on neural networks, its performance depends on how well the selected features can distinguish among fault classes. As a result, choosing proper wavelet function and wavelet coefficients is critical to the system performance. Since one can not make these choices with absolute certainty *a priori*, any additional analysis to ensure the distinctiveness of the selected features across fault classes is beneficial [13]. The test that will eventually determine the appropriateness of the selected wavelet function and features is the training phase which must meet a reasonable error goal leading to a satisfactory performance of the neural network.

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Cascaded Parallel Oversampling Sigma-Delta Modulators

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Abstract—Based on the well-known time-interleaved modulator (TIM), a new cascade-parallel architecture of oversampling sigma-delta analog-to-digital converters is proposed. While retaining the speed advantage of TIM, the new architecture gives a general method to effectively suppress the influence of circuit nonidealities, especially coefficient mismatches, on the converter's resolution. Such influence is a serious problem in the practical realization of TIM. Simulation results of examples of both TIM and the new architecture are given for comparison. In addition to its improved performance, the new architecture turns out to be quite simple. Therefore it can be a practical approach to extend the use of sigma-delta analog-to-digital conversion to high-speed applications.

Index Terms—Cascade, converters, parallel, TIM.

I. INTRODUCTION

Because of their outstanding linearity, oversampling converters have become a popular technique for data conversion [2]. However, due to the nature of oversampling, these converters are much slower than their Nyquist-rate counterparts. Hence, the applications of sigma-delta modulators are usually restricted to low-speed high-linearity applications such as digital audio. Emerging needs have forced designers to seek highly linear converters with broader input bandwidths.

Manuscript received January 1999; revised October 1999. This paper was recommended by Associate Editor H. Tanimoto.

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Publisher Item Identifier S 1057-7130(00)01463-4.

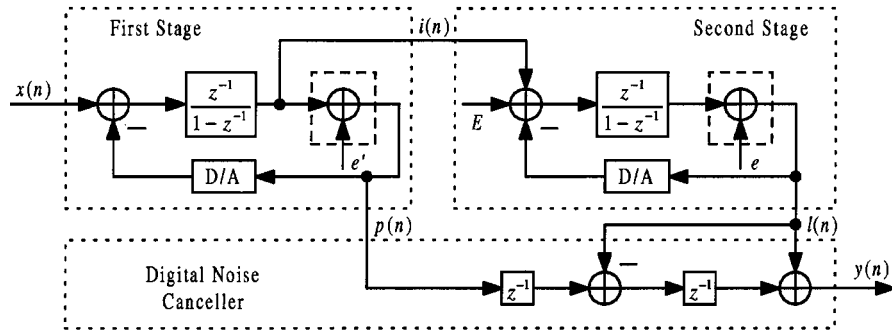


Fig. 1. (1-1) cascade.

One approach is to use high-order modulators and low oversampling ratios, but the complexity of such converter's antialiasing and decimation filters will increase with the order of the modulator.

Recently, several papers have utilized the concept of multirate signal processing [3], [4]. Reference [1] presented the time-interleaved modulator (TIM) structure which, by using M interconnected modulators working in parallel with each running at the same clock, raises the effective sampling rate to M times the clock speed of each modulator. In other words, high sampling rate could be achieved by increasing the number of modulators. Hence, we can obtain the desirable resolution without using a faster and more costly fabrication process or a higher order modulator.

In this brief, based on TIM, a new cascade-parallel architecture of sigma-delta analog-to-digital converters (ADC's) is proposed to give a general method to suppress the otherwise considerable effect of circuit nonidealities, especially coefficient mismatches, on the resolution of the converter, while at the same time retaining the speed advantage of TIM.

The outline of this brief is as follows. In Section II, first, the analysis of the sensitivity of TIM to coefficient mismatches is reviewed. Second, the cascade-parallel architecture is derived from a (1-1) cascade and then extended to general situations. Section III gives the simulation results for the comparison of the new architecture with TIM. Section IV addresses five practical issues regarding the implementation of the new architecture. Conclusions are given in Section V.

II. CASCADE-PARALLEL ARCHITECTURE

A. Coefficient Mismatches

In the circuit implementation of TIM, the effects of circuit nonidealities on the performance should be considered. Coefficient mismatches among parallel modulators in the TIM structure, according to the analysis in [1], cause the overall structure to become time varying and hence aliasing occurs. Those portions of the spectrum around $2\pi i/M$ ($i = 1, 2, \dots, M-1$) will get first attenuated and then folded back into the band of interest. This results in a flattening of the noise floor in the band of interest and a decrease of signal-to-noise ratio (SNR). Reference [1] mentioned that if $M = 2$, the dynamic range of a second-order TIM structure will fall to be nearly equal to that of the conventional modulator when there exists 0.1% coefficient mismatch.

Since TIM is so sensitive to coefficient mismatches that its speed advantage may be lost under the nonideal condition, it is necessary to find a general way to overcome this shortcoming before TIM can be used in practical applications. Reference [1] proposed a method called k-factor technique, which adjusted the coefficients in the transfer-function matrix slightly to generate notches in the spectrum portions that would be folded into the band of interest. However, the authors only gave an example of $M = 2$ and admitted that "the practical realization

of time-interleaved modulators with $M > 2$, would be a challenging task."

B. A Particularity of Cascaded Sigma-Delta Modulators

The conventional sigma-delta modulators are described as single loop [5]. Cascaded sigma-delta modulators consist of a cascade of several lower order single-loop modulators. Each of them converts the quantization error of the preceding modulator. The errors of all but the last modulator are then digitally cancelled. The noise introduced into the last stage will be shaped by the digital noise canceller before it appears as a portion of the converter's ultimate output. The shaping order is equivalent to the sum of the order of all the previous stages.

Take the (1-1) cascade shown in Fig. 1 as an example. Ideally, its modulating effect is equivalent to that of a single-loop second-order modulator [5]. Let e' denote the quantization error of the first modulator, e that of the second modulator and E the noise introduced into the second stage by factors other than quantization error, we have

$$\begin{aligned} i(n) &= x(n-1) - e'(n-1) \\ l(n) &= i(n-1) + E(n-1) + [e(n) - e(n-1)] \\ &= x(n-2) - e'(n-2) + E(n-1) + [e(n) - e(n-1)] \\ p(n) &= x(n-1) + [e'(n) - e'(n-1)] \\ y(n) &= p(n-2) + [l(n) - l(n-1)] \\ &= x(n-2) + [e(n) - 2e(n-1) + e(n-2)] \\ &\quad + [E(n-1) - E(n-2)]. \end{aligned} \quad (1)$$

The portion caused by E in $y(n)$ turns out to be $[E(n-1) - E(n-2)]$. In other words, it is shaped by the digital noise canceller for first order, equivalent to the first stage's order.

Replacing the last stage of a cascade with TIM, we obtain a new cascade-parallel architecture of sigma-delta ADC's. The TIM structure promotes the speed of the last stage while the effect of the noise introduced by coefficient mismatches is suppressed by the shaping of the digital noise canceller. To form the new architecture, we replace the second stage in Fig. 1 with the equivalent first-order TIM with $M = 4$, as shown in Fig. 2.

The detail of the transfer function matrix in Fig. 2 is shown in (2)

$$\begin{bmatrix} n_1 \\ n_2 \\ n_3 \\ n_4 \end{bmatrix} = \begin{bmatrix} z^{-1} & 1 & 1 & 1 \\ z^{-1} & z^{-1} & 1 & 1 \\ z^{-1} & z^{-1} & z^{-1} & 1 \\ z^{-1} & z^{-1} & z^{-1} & z^{-1} \end{bmatrix} \begin{bmatrix} m_1 \\ m_2 \\ m_3 \\ m_4 \end{bmatrix}. \quad (2)$$

C. Special Design for the First Stage

To cooperate with the second stage and promote the speed of the whole cascade, the first stage must also be a certain kind of parallel

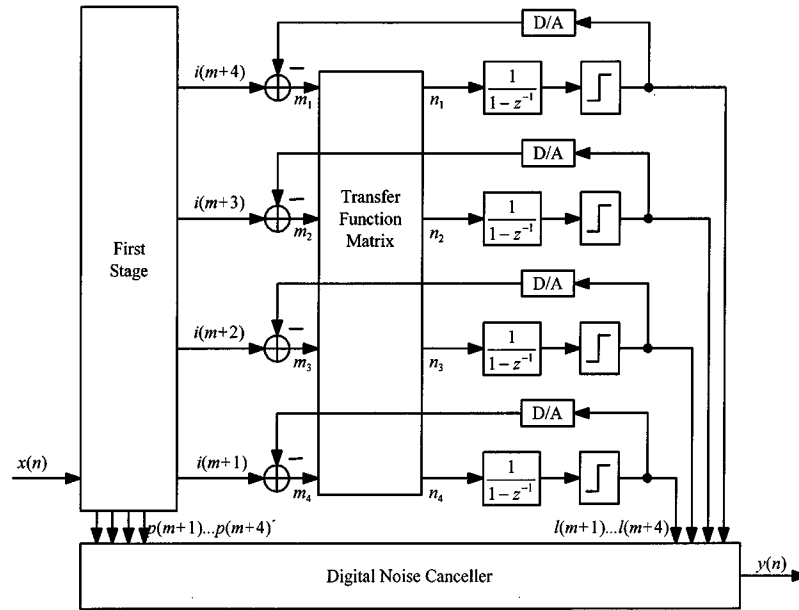


Fig. 2. An example of the cascade-parallel architecture.

structure whose effective sampling rate is four times its clock speed. Because of the shaping nature of the cascade, the architecture will inevitably be sensitive to coefficient mismatches if another TIM structure is adopted as the first stage.

So we modify the conventional first-order sigma-delta modulator to form a special design for the first stage. First, an interpolator is added to the input port of the conventional modulator, as is shown in Fig. 3. The interpolator evenly interpolates three zero values between every two successive input samples, thus raising the sampling rate to four times its original. Letting $x'(m)$ denote the interpolated input, we have

$$i(m+1) = i(m) + x'(m) - p(m). \quad (3)$$

Suppose m and n represent the same time, then $x'(m) = x(n)$ and $x'(m+1) = x'(m+2) = x'(m+3) = 0$, therefore

$$i(m+k) = i(m+k-1) - p(m+k-1), \quad \text{when } k=2,3,4. \quad (4)$$

Note that in (3) and (4), $p(m)$ represents the output of the internal digital-to-analog converter (DAC), i.e., an analog signal rather than a digital quantity.

To prevent the quantizer from overloading, the input amplitude is restricted to $(-L, +L)$ [5], where $\pm L$ are the output levels of the quantizer. Simulation results show that $i(m)$ will be in the range of $(-2L, +2L)$. Divide this range into four sub-ranges, and from (4), we obtain the different results of $p(m+k)$ ($k=1,2,3,4$), corresponding to $i(m+1)$ in different sub-ranges, which are shown in Table I. Note that all the signals have been normalized by L . Introduce three boolean variables: a , b , and c , which can only assume $+1$ and -1 . Suppose

$$a = \begin{cases} 1, & \text{when } 2 > i(m+1) > -1 \\ -1, & \text{when } -2 < i(m+1) < -1 \end{cases}$$

$$b = \begin{cases} 1, & \text{when } 2 > i(m+1) > 0 \\ -1, & \text{when } -2 < i(m+1) < 0 \end{cases}$$

$$c = \begin{cases} 1, & \text{when } 2 > i(m+1) > 1 \\ -1, & \text{when } -2 < i(m+1) < 1 \end{cases}$$

From the results in Table I, we can deduce

$$\begin{aligned} p(m+2) &= a(b \odot c), & p(m+3) &= -p(m+2) \\ p(m+4) &= -p(m+3). \end{aligned} \quad (5)$$

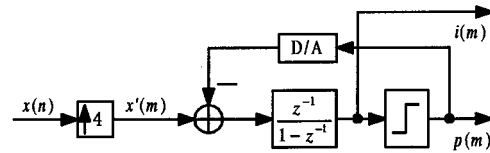


Fig. 3. The equivalent form of the first stage in Fig. 2.

TABLE I
DIFFERENT RESULTS OF $P(m+k)$ CORRESPONDING TO $i(m+1)$ IN DIFFERENT SUB-RANGES

The range of $i(m+1)$	Corresponding $p(m+k)$ ($k=1,2,3,4$)			
	$p(m+1)$	$p(m+2)$	$p(m+3)$	$p(m+4)$
$\in (-2, -1)$	-1	-1	+1	-1
$\in (-1, 0)$	-1	+1	-1	+1
$\in (0, +1)$	+1	-1	+1	-1
$\in (+1, +2)$	+1	+1	-1	+1

From (4) and (5), we find that $p(m+k)$ ($k=2,3,4$) and $i(m+k)$ ($k=2,3,4$) can be predicted simply according to $i(m+1)$. Since the interpolated zero values have no effect on the output of the integrator in Fig. 3, they do not really need to exist, i.e., the interpolator can be omitted. Moreover, $p(m+k)$ ($k=1,2,3,4$) can be summed and feedback together through a tri-value DAC. Hence, the analog circuit only needs to operate under a sampling rate which is a quarter of the effective sampling rate. Based on the idea, a special design for the first stage of the cascade-parallel architecture is proposed, as shown in Fig. 4. The outputs corresponding to the zero inputs are obtained through a predicting circuit made up of some comparators and logic gates. The output values of the tri-value DAC are $+2L$, 0 , or $-2L$.

D. Cascaded Parallel Sigma-Delta Modulator

Now a complete example of the cascade-parallel architecture has been obtained. The detailed structure of the digital noise canceller can be easily constructed on the basis of the one in Fig. 1. The new architecture can be generalized. For instance, M can assume values other than four and the order of the second stage can be arbitrary. There is no

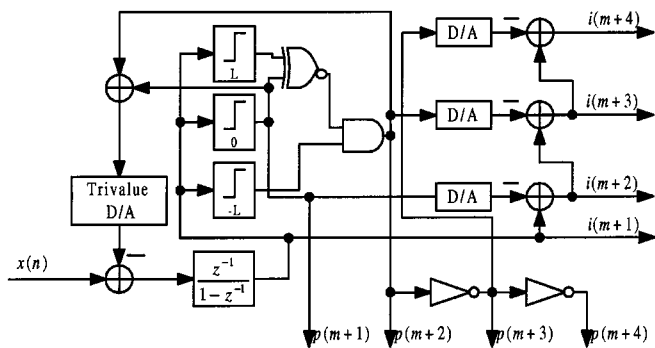


Fig. 4. Special design for the first stage.

theoretical limitation on them, but the first stage should be restricted to first order.

Interpolating will decrease the power of the input signal. The loss is $6 \log_2 M$ dB, and has nothing to do with the overall order of the system and the sampling rate. Since the new architecture has an effective sampling rate at M times its sampling rate, the noise power in the signal band is $6(K + 0.5) \log_2 M$ -dB lower than that of the conventional modulator if both are of the same order and sampling rate [5], where K denotes their order. So the cascade-parallel architecture has an SNR $6(K - 0.5) \log_2 M$ -dB better than the conventional modulator under the same conditions. In the example of Fig. 2, it is 18 dB, which means that if the resolution requirements for the new architecture and the conventional second-order modulator are the same, the former will have a bandwidth more than twice that of the latter.

One problem worthy of attention is that, according to the theoretical deduction, the images caused by up-sampling, i.e. interpolating, will appear intact in the ultimate output. Since it has to cope with these images, the digital decimation filter after the new architecture has to become more complex.

III. SIMULATION RESULTS

We use SIMULINK [6] to carry out simulations. The quantizer output levels are $\pm L$, $L = 1$. The input is a sinusoid with amplitude of 0.2 and a frequency of 1 kHz, the band of interest is assumed to be 0–2 kHz and the hanning window is used to process the output signal.

First, under ideal conditions, we compare the resolution of the new architecture in Fig. 2 with the conventional second-order modulator in [7]. The results are listed in Table II, we find that the analysis in Section II-C proves to be accurate. The architecture in Fig. 2 does have an 18-dB better SNR when both circuits operate at the same sampling rate.

Though ideally the SNR of a second-order TIM with $M = 4$ will be 12-dB better than that of the architecture in Fig. 2, the new architecture is insensitive to circuit nonidealities compared with TIM.

Fig. 5(a) shows the output signal power spectrum of both a second-order TIM ($M = 4$) and the architecture in Fig. 2 under ideal condition and 0.1% coefficient mismatches, respectively. Coefficient mismatches are simulated by setting gains (ideally one) of the four summing conjunctions in Fig. 2 to different values (slightly deviating from one) because simulations indicate that such kind of mismatches can cause much more signal-to-noise ratio (SNR) loss for TIM than mismatches among integrating ratios of the integrators can. The oversampling rate is set to 128. To eliminate tones in the output signal, ± 0.15 ditherings are applied to the second stage of the new architecture. Note that, unlike in Fig. 5(a), the noise floor in the band of interest in Fig.

TABLE II
COMPARISON OF SNR'S: THE CONVENTIONAL MODULATOR VERSUS THE CASCADE-PARALLEL ARCHITECTURE

Sampling Rate (kHz)	Oversampling Rate	SNR of the conventional second-order modulator (dB)	SNR of the new architecture in Fig.2 (dB)
128	32	48.9	68.0
256	64	65.8	84.5
512	128	78.2	97.4
1024	256	95.1	113.2

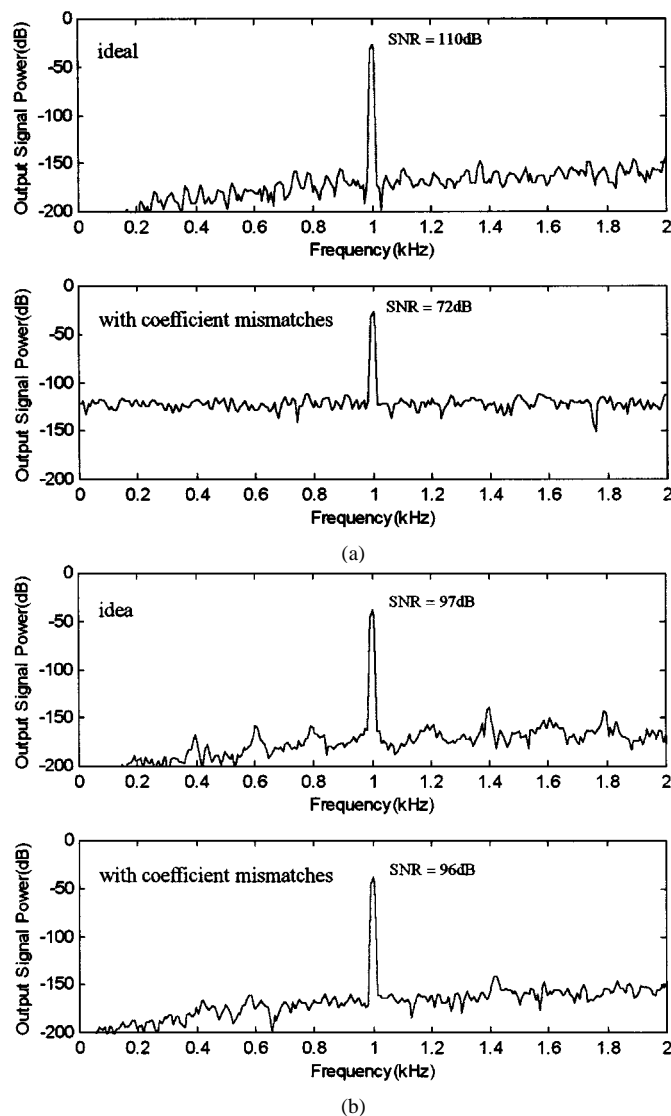


Fig. 5. (a) Output signal power spectrum of second-order TIM, $M = 4$ for both ideal condition and 0.1% coefficient mismatches. (b) Output signal power spectrum of the cascade-parallel architecture in Fig. 2 for both ideal condition and 0.1% coefficient mismatches.

5(b) has not been flattened, and the SNR only changes slightly from 97 to 96 dB, much better than that from 110 to 72 dB in Fig. 5(a).

There are also other nonidealities that may influence the resolution of TIM remarkably, such as the op-amp dc offset. The analysis of its effect

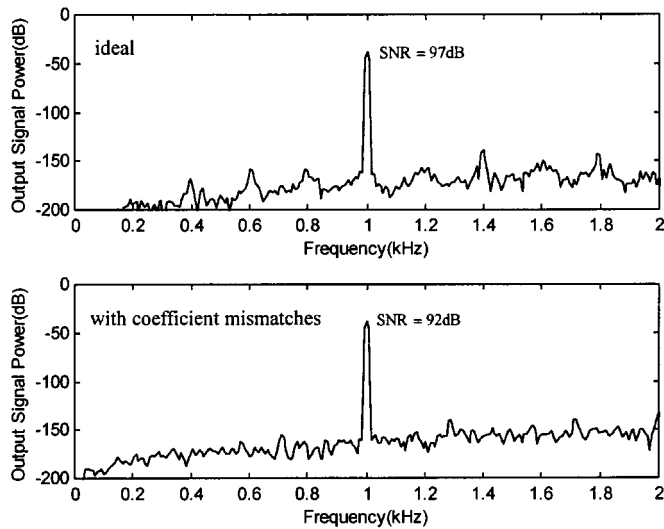


Fig. 6. Output signal power spectrum of the cascade-parallel architecture in Fig. 2 (top) under ideal condition and (bottom) with coefficient mismatches and op-amp dc offsets.

on the performance of the new architecture, as well as the simulation results, will be shown in Section IV-B.

IV. PRACTICAL ISSUES

A. Finite Gain of Operational Amplifier

Integrators are basic building blocks in a sigma-delta modulator. The overall converter performance is largely determined by the characteristics of the integrators, especially in the case of cascaded modulators. Because of noise shaping, only the characteristics of the integrator in the first stage are important for the performance of the cascade-parallel architecture.

Finite gain of op-amp will cause a pole error in the switched-capacitor (SC) integrator in the first modulator, which will result in the leakage of unshaped quantization noise to the output. This noise leakage may be the main performance limitation for cascaded modulators that employ a first-order loop as the first stage. Fortunately, [8] has already studied this problem when designing a (1-1-1) cascaded sigma-delta modulator. It gave a solution utilizing a special auto-zeroed integrator topology proposed by [9], which makes the gain of the op-amp almost squared.

B. Dc Offsets of Integrators in the Second Stage

Besides coefficient mismatches, another practical problem for TIM is the effect of op-amp dc offsets. As is described in [1], unless k -factor technology is utilized, TIM is unable to cancel these offsets, which may keep the outputs of the integrators increasing or decreasing and eventually cause the integrators to clip as well as the quantizers to overload thereby degrade noise shaping performance. But the application of k -factor technique will cause more SNR to be traded away for $M > 2$ [1].

However, when considering the influence of op-amp dc offsets on real circuits, we surely should take into account the finite gain of the op-amps, which changes the ideal transfer function of integrators

$$Y(z) = \frac{GX(z)}{(1-z^{-1})} \quad \text{into} \quad Y(z) = \frac{\frac{GA}{1+G+A}X(z)}{\left(1 - \frac{1+A}{1+G+A}z^{-1}\right)} \quad (6)$$

where A is the gain of the op-amp and G is the ratio of values of the charge capacitor and the integrating capacitor in the SC integrator. Equation (6) shows that the integrator's dc gain is a finite value A rather than infinity. Hence, the actual influence of dc offsets on the integrator will be limited. For instance, when the output of an integrator consisting of a 40-dB gain op-amp has already been up to 1 V, a +10-mV dc offset can no longer keep it increasing.

In addition, such influence, when it happens in the second stage of our new architecture, will also be shaped by the digital noise canceller for first order, which can greatly reduce its damage to the overall performance.

During simulation, the ideal integrator transfer function in Fig. 2 is replaced by (6) and A is assumed to be 80. Oversampling rate is set to 128. Keep $L = 1$ and a set of dc offsets, +0.003, -0.001, +0.006, and -0.007, are embedded, respectively, into the four channels of the second stage. Coefficient mismatches are retained. To eliminate tones in the output signal, ± 0.15 ditherings are applied to the second stage. Fig. 6 shows the final result. We can see the dc offsets, together with the coefficient mismatches, only cause a drop of SNR from 97 to 92 dB, which is slight and tolerable.

Moreover, when we need to further reduce the loss of SNR, the offset-free integrator presented in [10] can be utilized to cope with the problem of dc offsets more elaborately.

C. Non-Linearity of the Tri-Value DAC

The DAC in the first-stage modulator's feedback loop may be a multilevel one. But analyses, like those in Section II-C, indicate that the number of its output levels has no relations with the exact value of M and will never be more than three. The DAC must be tri-level when M is even and 1-bit (two output levels) when M is odd. In the case of Fig. 4 $M = 4$, so a tri-value DAC has been used.

A 1-bit DAC is inherently linear, but a tri-value one is not. So, when M is even, without being shaped, the nonlinearity of the tri-value D/A will directly limit the overall resolution of the system.

Output levels of the tri-value DAC are $+2L$, 0 and $-2L$, which can be seen as the results of $(+L)+(+L)$, $(+L)+(-L)$ and $(-L)+(-L)$. So practically, we can still use a 1-bit DAC, whose output levels are $\pm L$ in the feedback loop and raise the sampling rate of the first-stage integrator twice. By adding two successive outputs of the 1-bit DAC together to get a desired value, we obtain an equivalent tri-value DAC working at the normal sampling rate, whose linearity can be guaranteed by the inherent linearity of the 1-bit DAC.

D. Non-Linearity of the Three Comparators

There are three comparators, i.e., quantizers, in the first stage of the new architecture, and their threshold voltages are $-L$, 0 , and L , respectively. In other words, the threshold voltages are arranged linearly. But in practice, there will always be some nonlinearity among them because of the imprecise circuit. The effect of this nonlinearity is equivalent to introducing some noise into the input to the comparators. This noise will go with the quantization error to form e' in Fig. 1. It is shown in (1) that e' does not appear in the ultimate output of (1-1) cascade. Therefore, theoretically, the nonlinearity of these three comparators can not influence the converter's resolution at all. Even in real circuits, where exists the leakage of e' to the output because of finite gain of the op-amp, the negative effect of this nonlinearity will not be serious after the method mentioned in Section IV-A is adopted.

E. Mismatches Among the DAC's

There are several DAC's, not including the tri-value one, in the first stage of the new architecture. The effect of mismatches among these DAC's is equivalent to introduce noise into the second stage; that is, it

can be seen as part of E in Fig. 1, so it will be shaped by the digital noise canceller for first order, as shown in (1), and will thereby be effectively suppressed, too.

V. CONCLUSION

The analysis of the sensitivity of TIM to coefficient mismatches has been reviewed. A new cascade-parallel architecture of sigma-delta ADC's is proposed on the basis of TIM. Though the derivation procedure of it is based on an example of (1-1) cascade and M is assumed to be four, the cascade-parallel architecture can be a general method to overcome the shortcoming of TIM through extensions. Simulation results of the examples indicated that the new architecture effectively suppresses the influence of the noise introduced by coefficient mismatches, while retaining the speed advantages of TIM. In addition, it turned out to be quite simple. Thus, it can be a good approach to implement TIM in practical applications.

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Time-Scaled Electrical Networks—Properties and Applications in the Design of Programmable Analog Filters

Shanthi Pavan and Yannis Tsvividis

Abstract—In this paper, we discuss the properties of time-scaled electrical networks. Two specific ways of implementing scaled linear networks, constant-conductance scaling and constant-capacitance scaling, are reviewed along with their noise properties. We then extend time scaling to nonlinear networks. We show that constant-capacitance scaled networks are optimal with respect to noise and dynamic range, irrespective of the scaling factor.

Index Terms—Continuous time, filter, nonlinear networks, programmable.

I. INTRODUCTION

Continuous-time integrated filters need to be programmable over wide frequency ranges for several applications, e.g., in the read channel of hard disk drives. Such filters must maintain the relative shape of the frequency response identical, irrespective of the set bandwidth, while maintaining adequate dynamic range. Approaches to the design of programmable filters are considered in this brief.

A. Time Scaling: Definition

We will discuss both linear and nonlinear networks. Since, in the latter, the term "frequency response" does not have meaning in the strict sense of the term, we will use the term "time scaling" rather than "frequency scaling" throughout this paper.

Consider an initially relaxed network \mathcal{N} . For the time being, we consider a single input, single output network. Let an arbitrary input voltage $v_i(t)$ produce an output voltage $v_o(t)$. Further, let us assume the existence of a network $\hat{\mathcal{N}}$ satisfying the following condition: Any input $\hat{v}_i(t) = v_i(\alpha t)$ results in an output $\hat{v}_o(t) = v_o(\alpha t)$. The only restriction on α is that it be positive. Then, we call $\hat{\mathcal{N}}$ the time-scaled version of \mathcal{N} , with a scaling factor α . This is denoted in Fig. 1. When \mathcal{N} and $\hat{\mathcal{N}}$ are linear, scaling in time by α corresponds to scaling of the frequency response of the network by $1/\alpha$. *The relative shape of the magnitude response remains the same.*

Throughout this paper, we discuss only (trans)conductance-capacitance networks, due to their significance in practical filter designs (for example, the disk-drive-read channel application). Extension to active-RC networks is easy and is not considered in this work. Two methods for realizing time (frequency-response) scaled networks are (Fig. 2) [1] the following.

- 1) Constant-capacitance scaling: multiply *all* conductances and transconductances by α , while keeping all capacitors unchanged.
- 2) Constant-conductance scaling: multiply *all* capacitors by $1/\alpha$, while keeping all conductances and transconductances unchanged.

The above two scaling techniques are not the only possibilities. For instance, one could easily think of a strategy where all conductances are

Manuscript received June 1999; revised October 1999. This paper was recommended by Associate Editor F. Maloberti.

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Publisher Item Identifier S 1057-7130(00)01459-2.