Schuyler **Eldridge**

computer engineer

contact

schuye@bu.edu
+1 (914) 382 1315
US Citizen

seldridge.github.io
github.com/seldridge

hardware

Chisel
Verilog/SystemVerilog

software

Assembly (x86, RISC-V)
Bash
C/C++
GNU Make
Java
LaTeX
Matlab
Perl
Python
Scala
TCL

tools

Cadence RTL Compiler
Cadence SoC Encounter
Emacs
Gem5
Git
GTKWave
Icarus Verilog
Jenkins
Linux
Modelsim
Xilinx ISE/Vivado

coursework

Advanced Data Structures
Computer Architecture
Control Systems
Digital Design in Verilog
Digital Signal Processing
High Performance Programming
Microprocessors
VLSI

education

2010–2016 **Ph.D** Computer Engineering — Boston University

Thesis: *Viable Neuromorphic Computing via Neural Network Accelerators*

Design, implementation, and management of neural network accelerators for general use, approximate computing, and prediction of microprocessor state

- Designed a fixed topology neural network accelerator for mathematical function approximation
  - Implemented in **Verilog**
  - Evaluated for energy-efficiency with a **Cadence** ASIC tooflow
- Designed a multi-transaction, arbitrary topology neural network accelerator
  - Modeled in **C++** and integrated and tested with **gem5**
  - Implemented in both **SystemVerilog** and **Chisel**
  - Integrated as a coprocessor of a **RISC-V** microprocessor
  - Interfaced with user and kernel via libraries in **C** and **RISC-V Assembly**
  - Evaluated on a **Xilinx FPGA** platform
- Setup and managed an automated testing server running **Jenkins**

Biologically-Inspired Optical Flow on FPGA

Implementation of a biologically inspired optical flow algorithm on FPGA

- Reverse engineered a camera interface to capture consecutive frames of real-time video
- Computed optical flow by shifting one image with respect to the other, filtering both with a Gabor filter bank, and correlating the results
- Designed linear interpolation, square root, division, and CORDIC units as well as associated state machines in **Verilog**
- Wrote a custom **Verilog** UART transmitter/receiver and interfaced this system with **Matlab**

2006–2010 **BS** Electrical Engineering — Boston University

Summa Cum Laude – GPA 3.85/4.0

- Senior Design Project: PID-controlled Object Tracking System on FPGA and DSP
- Frogger clone in **Verilog** running on FPGA
- 32-bit MIPS 5-stage pipelined CPU in **Verilog**

experience

Summers 2013–2015 **NASA Jet Propulsion Lab** — Pasadena, CA

Space Technology Research Fellow

Performed neural network accelerator research focusing on their potential for fault tolerance (2013), design of a neural network accelerator simulator in **C++** (2014), and migration of a **SystemVerilog** hardware implementation to **Chisel** (2015)

Summer 2011 **Intel Corporation** — Hudson, MA

Graduate Technical Intern

Wrote tests to verify the functionality of memory controllers in **SystemVerilog** as part of the Xeon server group

Summer 2010 **Intel Corporation** — Hudson, MA

Graduate Technical Intern

Designed and optimized hashing functions in **x86 assembly** while evaluating functions for quality

awards

2012–2016 **Space Technology Research Fellowship** NASA
Four year NASA fellowship titled *Biologically-Inspired Hardware for Land/Aerial Robots*. This award has included yearly on-sites at NASA facilities.

2012 **CELEST/CompNet Award** Boston University
Awarded at Boston University's Science Day for work titled *Biologically-Inspired Hardware for Autonomous Robots*

2010 **Boston University Dean's Fellowship** Boston University
Full scholarship merit award for first year Ph.D students

2010 **P. T. Hsu Memorial Award for Outstanding Senior Design Project** Boston University
Awarded to the best senior design project team

2006–2010 **Boston University Engineering Scholar Award** Boston University
Undergraduate merit award with half-tuition scholarship

interests

Former nationally competitive figure skater

- 2007 US National competitor
- 2004–2010 Eastern Sectional competitor
- 2007–2015 Intercollegiate Team competitor representing Boston University, National Champions 2009–2010

publications

conference and workshop publications

Towards General-Purpose Neural Network Computing
S. Eldridge, A. Waterland, M. Seltzer, J. Appavoo, A. Joshi
Proceedings of the International Conference on Parallel Architectures and Compilation Techniques, 2015

Exploiting Hidden Layer Modular Redundancy for Fault-Tolerance in Neural Network Accelerators
S. Eldridge, A. Joshi
Boston Area Architecture Conference, 2015

Programmable Smart Machines: A Hybrid Neuromorphic Approach to General Purpose Computation
J. Appavoo, A. Waterland, S. Eldridge, K. Zhao, A. Joshi, S. Homer, M. Seltzer
NeuroArch Workshop, 2014

Neural Network-Based Accelerators for Transcendental Function Approximation
S. Eldridge, F. Raudies, D. Zou, A. Joshi
Proceedings of the Great Lakes Symposium on VLSI, 2014

Approximate Computation using a Neuralized Floating Point Unit
S. Eldridge, F. Raudies, A. Joshi
Brain Inspired Computing Workshop, 2013

articles

Learning to Navigate in a Virtual World using Optic Flow and Stereo Disparity Signals
F. Raudies, S. Eldridge, A. Joshi, M. Versace
Artificial Life and Robotics 19.2 (2014) pp. 157–169. Springer, 2014

tech reports

Reinforcement Learning of Visual Navigation Using Distances Extracted from Stereo Disparity or Optic Flow
F. Raudies, S. Eldridge, A. Joshi, M. Versace
BU/ECE-2013-1, 2013

patents and patent applications

Digest Generation
V. Gopal, J. D. Guilford, S. Eldridge, G. M. Wolrich, E. Ozturk, W. K. Feghali
US Patent Application 13/995,236, 2011