# Forming Electrical Networks in Three Dimensions by Self-Assembly

**David H. Gracias, Joe Tien, Tricia L. Breen, Carey Hsu, George M. Whitesides***

**Self-assembly of millimeter-scale polyhedra, with surfaces patterned with solder dots, wires, and light-emitting diodes, generated electrically functional, three-dimensional networks. The patterns of dots and wires controlled the structure of the networks formed; both parallel and serial connections were generated.**

Most fabrication of microelectronic devices is carried out by photolithography and is intrinsically two-dimensional (2D) (*1*). The 3D interconnections required in current devices are fabricated by the superposition of stacked, parallel planes and by their connection using perpendicular vias (*2–4*). We demonstrate self-assembly as a strategy to form interconnections between electronic devices and prefabricated circuits, and to form 3D electrical circuits.

Previous uses of self-assembly to fabricate electronic devices include shape-directed fluidic self-assembly of light-emitting diodes (LEDs) on silicon substrates (*5*) and coplanar integration of segmented integrated circuit (IC) devices (*6*) into 2D "superchips" using capillary forces at the surface of a flotation liquid (*7*). We demonstrate the formation of two classes of 3D electrical networks—parallel and serial—by self-assembly, as an early step toward a strategy for fabricating 3D microelectronic devices. The basic unit in these assemblies is a polyhedron [a truncated octahedron (TO)], on whose faces electrical circuits are printed. In the present demonstrations, these circuits include LEDs to demonstrate electrical connectivity and trace the networks; in the future, they will include devices with more complex functionality (e.g., processors). The LEDs are wired to patterns of solder dots on adjacent faces of the polyhedron. The TOs are suspended in an approximately isodense liquid at a temperature above the melting point of the solder (m.p. ~ 47°C), and allowed to tumble gently into contact with one another. The drops of molten solder fuse, and the minimization of their interfacial free energy generates the forces that assemble the TOs into regular structures (*8*). Processes based on capillary interactions between solder drops have been used previously to assemble electronic and mechanical structures: examples include "flip-chip" technology (*9*) and the rotation of parts of microstructures into nonplanar orientations (*10, 11*). During assembly, recognition of the pattern of dots on one face by that on another orients and registers the patterns, and generates dot-on-dot electrical connections among polyhedra. Self-assembly of polyhedra can generate networks in which the LEDs are connected either in parallel or in series. Figure 1 outlines both the fabrication of the patterned polyhedra and their self-assembly into 3D structures that include electrical networks (*12*).

We used a scheme in which LEDs were mounted on the hexagonal faces of the TO, and the solder dots were placed on the square faces. To maximize the rate of self-assembly, all of the square faces of the TO had the same fourfold symmetric pattern of solder dots. With this pattern, correct registration of patterns on juxtaposed faces occurred in one of four indistinguishable ways; dots on the patterns that transformed into each other under fourfold rotational symmetry were equivalent and served the same function. On the 3 mm by 3 mm square face, the width of all of the solder dots was ~1 mm (Fig. 2). A common size was required: the solder wetted the copper with a well-defined contact angle, and each drop of the same size therefore had the same height. Empirical testing suggested that the optimum distance between adjacent solder dots was approximately one-half their width. Smaller separations resulted in electrical shorting between dots due to bridging with solder; larger separations resulted in misalignment. We designed the shapes of solder dots to give an energy diagram for self-assembly having one large (global) minimum and relatively small local minima.

The wires that connect different solder dots electrically on each TO were fabricated in the same way as the dots. When the patterned TOs were dipped in solder, these wires were also covered with a solder layer. By making the wires substantially narrower (~150 μm) than the diameter of the dots (~1 mm), we limited the height of the solder film on the wires to ~15% that of the dots. When the faces self-assembled, the larger dots fused into connections, but the smaller wires did not touch and fuse (Fig. 2C). It was, as a result, unnecessary to insulate the wires to prevent shorting, even when they crossed on juxtaposed faces of two TOs.

We wished to demonstrate, by self-assembly in 3D, networks that are widely used in current 2D IC technology. In these systems, pins on processors belong to one of three groups: bus lines (driving voltage, clock), inputs, and outputs. Bus lines connect processors in parallel; outputs of one processor connect serially to inputs of adjacent processors.

In the pattern of solder dots (Fig. 2D), the five dots that lie on reflection axes comprise

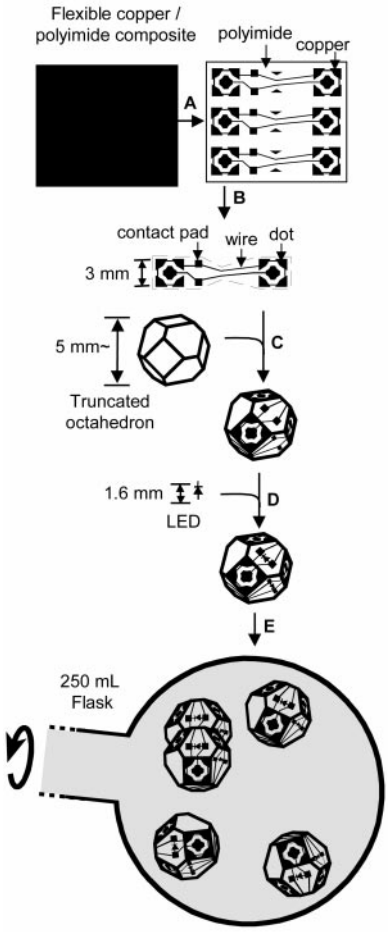


**Fig. 1.** The procedure used to form electrical networks in 3D by self-assembly (*12*). (**A**) An array of the basic pattern of copper dots, contact pads, and wires was defined on a flexible copper-polyimide sheet using photolithography and etching. (**B**) These pattern elements were cut out along the dotted line, (**C**) glued on the faces of the polyhedron, and (**D**) LEDs were soldered manually onto the contact pads. (**E**) The copper dots and wires on the TOs were coated with solder, and self-assembly occurred in hot, isodense, aqueous KBr solution.

Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138, USA.

*To whom correspondence should be addressed. E-mail: gwhitesides@gmwgroup.harvard.edu

two sets of dots differentiated by symmetry: {1} and {2, 5, 8, and 11}. During self-assembly, dots from one set on a TO connect to dots from the same set on another TO. These dots are used for parallel or bus-line connections. The other dots, {3, 6, 9, and 12} and {4, 7, 10, and 13}, form two distinct sets related by reflection symmetry. Upon assembly, dots from one set on a TO (e.g., outputs from one processor) connect to those from the other set on another TO (e.g., inputs to a second processor). These dots are used for serial, input/output connections.

Figure 3 shows the realization of a 3D network with parallel connectivity, using self-assembly. The pattern of solder dots consisted of dots {2, 5, 8, and 11} and {1} (Fig. 2D), which were on the axes of symmetry of the square face (*13*). In the assembled aggregate, LEDs on one TO connected to those on the adjacent TO in parallel, along three orthogonal directions. The fidelity of the interconnections was visualized by lighting up the LEDs connected in parallel in the assembly.

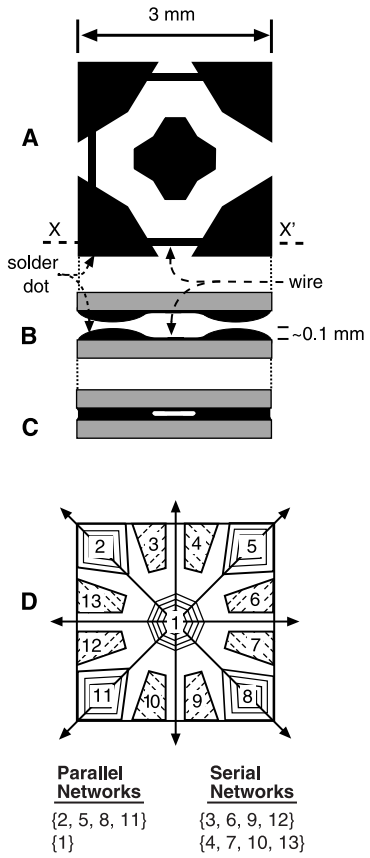


**Fig. 2.** Strategies used to design patterns of solder dots. (**A**) The widths of all the dots in the patterns used were approximately the same. The width of the wires was smaller. (**B**) A cross-sectional view [section XX′ in (A)] of two assembling faces. (**C**) When the faces connect, the solder dots fuse with each other, whereas the wires between them do not touch. (**D**) A pattern comprising dots that can be used for both parallel and serial networks.

This self-assembled, 3D parallel network mimicked bus lines in circuits in which a number of electrical components are powered by the same common wires.

For the realization of a 3D network with serial connectivity (Fig. 4), we used the sets of solder dots {3, 6, 9, and 12} and {4, 7, 10, and 13} (Fig. 2D) that were off the axes of symmetry of the square face (*14*). The important feature of the assembled 3D network was that the cathode of one LED always connected to the anode of another LED across the assembling faces. The serial networks were traced by illuminating sets of LEDs (e.g., Fig. 4D) (*15*).

The 3D assemblies can be designed to be porous: this porosity may allow for cooling fluid to be pumped through the assemblies. The shape and the distribution of solder dots on the assembling faces raises interesting questions regarding the design of patterns that best enable the "recognition" of one pattern by another. Other concepts adapted from 2D self-assembly, such as hierarchical self-assembly (*16*) and shape-selective self-assembly [that is, use of lock-and-key structures (*17, 18*)], offer more sophisticated strategies for the fabrication of asymmetrical networks incorporating more than one repeating unit.

We have demonstrated parallel and serial connectivity separately; it is possible to extend these ideas to more complex networks involving different combinations of parallel and serial connections. The LEDs in our demonstrations are simple bipolar electronic de-

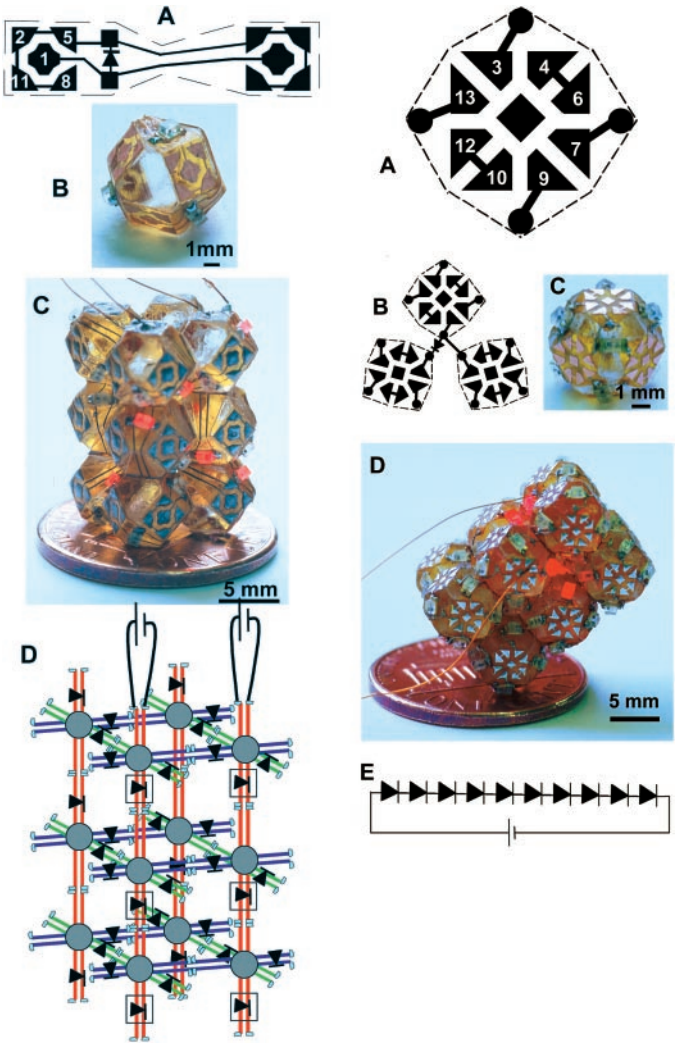


**Fig. 3 (left).** A self-assembled 2 × 2 × 3 aggregate containing 12 TOs and demonstrating parallel connectivity. (**A**) The pattern of copper dots, wires, and contact pads used. (**B**) A patterned TO with three LEDs, prior to assembly. (**C**) A photograph of the self-assembled aggregate and a penny (to indicate size). Two electrically isolated pairs of wires connected to a battery illuminate six LEDs in an electrically continuous loop involving three TOs. (**D**) Circuit diagram showing the parallel network formed. The gray circles represent individual TOs. The blue half-circles represent solder dots that connect on juxtaposed faces of two TOs. The LEDs are shown in black. The network contains 16 pairs of wires, which consist of four (red), six (green), and six (blue) pairs in each of the three dimensions. The six LEDs that illuminate are highlighted by black squares **Fig. 4 (right).** A self-assembled 2 × 2 × 3 aggregate containing 12 TOs and demonstrating serial connectivity. (**A**) The pattern of solder dots used. (**B**) The terminals of a single LED are directly soldered across two contact pads, and a wire is soldered in a way that connects the third contact pad to one of the terminals of the LED, using a polarity in which the anode of the LED connects to dots from the set {3 and 9} and the cathode connects to dots from the set {7 and 13}. (**C**) A patterned TO prior to assembly. (**D**) A self-assembled aggregate. The LEDs on different TOs connect to each other in serial loops. The loops were traced by powering pairs of leads. Individual loops range in size from those containing two LEDs to one that contains 10 LEDs; this loop is shown illuminated. (**E**) The circuit diagram sketching the largest serial loop formed; 10 LEDs illuminate when the loop is connected to a battery (D). The LEDs connect cathode to anode in all loops.

vices; to fabricate 3D computational devices, we must incorporate elements of digital logic [e.g., five-pin, single-logic gates (*19*)]. Self-assembly facilitates the formation of highly interconnected elements in both deterministic and probabilistic networks; it may be possible to use this kind of self-assembly to generate other logical structures (e.g., artificial neural networks) (*20*).

We have carried out all experiments using only a limited number of polyhedra: to extend this approach to a larger number of elements, and to smaller elements, it will be necessary to develop practical methods for fabricating these elements; the need for 3D microfabrication permeates 3D self-assembly, but new methods are beginning to emerge (*21–24*). Although large arrays may have defects, it may be possible to develop computational algorithms even in defective networks (*25–28*).

**References and Notes**


1. S. A. Campbell, *The Science and Engineering of Microelectronic Fabrication* (Oxford Univ. Press, New York, 1996).
2. S. K. Gandhi, *VLSI Fabrication Principles* (Wiley, New York, ed. 2, 1994).
3. W. Maly, *Atlas of IC Technologies: An Introduction to VLSI Processes* (Benjamin-Cummings, Menlo Park, CA, 1987).
4. P. M. Zavracky, M. Zavracky, V. Duy-Phach, B. Dingle, U.S. Patent 5,976,953 (1999).
5. H. J. Yeh and J. S. Smith, *IEEE Photonics Technol. Lett.* **6**, 706 (1994).
6. C. D. Fung, P. W. Cheung, W. H. Ko, D. G. Fleming, Eds., *Micromachining and Micropackaging of Transducers* (Elsevier, Amsterdam, 1985).
7. J. W. Sliwa Jr., U.S. Patent 5,075,253 (1991).
8. T. L. Breen, J. Tien, S. R. J. Olivier, T. Hadzic, G. M. Whitesides, *Science* **284**, 948 (1999).
9. L. F. Miller, *IBM J. Res. Dev.* **13**, 239 (May 1969).
10. R. R. A. Syms and E. M. Yeatman, *Electron. Lett.* **29**, 662 (1993).
11. F. K. Harsh, V. M. Bright, Y. C. Lee, *Sens. Actuators A* **77**, 237 (1999).
12. Masters for forming the polyhedra were machined out of aluminum, and molds were made from these masters using poly(dimethyl siloxane) (PDMS Sylgard 184, Dow Corning). Polymeric polyhedra were then cast in these molds, using a photocurable polymer (NOA 73, Norland). A sheet of flexible copper-polyimide composite (Pyralux LF 9110, DuPont) was coated with a photoresist (Microposit, 1813, Shipley), using hexamethyldimethylsiloxane (HMDS) as a primer. Both were spun on at 4000 rpm. After a soft-bake at 115°C for 5 min, this sheet was exposed to UV light through a negative mask containing an array of the pattern of connector dots, contact pads, and wires. The exposed photoresist was developed, and the exposed copper was removed by etching with an aqueous ferric chloride solution (1.4 g of $FeCl_3$ per milliliter of $H_2O$). Unexposed photoresist was removed with acetone. The basic pattern was then cut out manually and glued (Krazy Glue, Elmer's Products) to the faces of the polyhedra. In the demonstrations of parallel and serial networks, LEDs (BL-HS136, American Bright Optoelectronics) were manually soldered (Rosin Core Solder, Radio Shack, m.p. ~185°C) onto the copper contact pads. These soldered regions were coated with a thin impervious layer of adhesive (CA-50 Gel, 3M) to avoid wetting and cohesion of these regions during assembly. The adhesive was allowed to harden completely over 48 hours. The polyhedra were then immersed in a bismuth solder (117, Small Parts Inc., m.p. ~47°C), which was melted in an aqueous solution of hydrochloric acid (pH ~ 1). The acid dissolved the oxide layer on the copper and the solder. The solder coated only the exposed copper regions on the polyhedra (dots and wires), but did not wet the polymeric surfaces. The solder-coated polyhedra were allowed to self-assemble in an aqueous KBr solution [density of 1.1 to 1.4 g/cm$^3$, pH of 3 to 4, adjusted with acetic acid to dissolve oxides on the solder (a function similar to that of flux in conventional soldering) and ~0.001% (v/v) of detergent (Triton X-100, Aldrich) to prevent the formation of bubbles at the surface of the polyhedra] in an indented round-bottomed flask, heated above the melting point of the solder (~70°C) in an oil bath. The flask was placed horizontally on a rotary evaporator that was rotated at 5 to 20 rpm. All self-assemblies were complete within 1 hour. The assemblies were rotated for an average of 15 min after they formed, at which time the assembly was allowed to cool. We believe that the last 15 min may serve to anneal the structure to correct errors in the connections. On cooling, the molten solder interconnections solidified and gave the aggregates sufficient strength so that they could be manipulated.
13. Two electrically isolated wires connected the two sets. An LED was soldered on the contact pads between the wires, using a polarity in which the cathode was connected to the wire between dots {2, 5, 8, and 11}, and the anode was connected to the wire between dots {1} (Fig. 3A). The pattern was glued on the TO in such a way that the copper dots covered two opposite square faces, while the two wires ran across the two hexagonal faces between them.
14. In order to reduce the number of circuits that would be formed (and of LEDs required to check their electrical connectivity) and to minimize the geometrical problems of packing the LEDs in the arrays, only four of the dots (we call these dots "active") in the solder pattern ({3, 9} and {7, 13}) were wired to LEDs. The other four dots ({6, 12} and {4, 10}) in the pattern were connected to each other (we call these dots "passive"). A single TO contained eight LEDs, one on each of the hexagonal faces, with the square faces covered with the pattern of connector dots. The active and passive dots had twofold symmetry, while the global pattern on individual connector dots on the assembling square faces had fourfold symmetry. This difference in symmetry resulted in the formation of a stochastic network upon self-assembly [if a deterministic network were required, all the dots ({3, 6, 9, and 12} and {4, 7, 10, and 13}) would need to be connected to LEDs]. There are three types of connections which result from overlap of dots at each assembling face: (i) connections between LEDs on different TOs, involving only active dots with a probability of one-fourth; (ii) connections between LEDs on the same TO, involving both active and passive dots with a probability of one-half; and (iii) connections containing no LEDs, involving only passive dots with a probability of one-fourth.
15. In a bipolar, random system, the probability of the anode connecting to the cathode is one-half. For 10 LEDs to form a functional serial loop, the probability would be $1/2^9$ or 1/512.
16. I. S. Choi, N. Bowden, G. M. Whitesides, *Angew. Chem. Int. Ed. Engl.* **38**, 3078 (1999).
17. N. Bowden, A. Terfort, J. Carbeck, G. M. Whitesides, *Science* **276**, 233 (1997).
18. P. W. Rothemund, *Proc. Natl. Acad. Sci. U.S.A.* **97**, 984 (2000).
19. Five-pin, single-logic gates are part of the "Little Logic" line of products sold by Texas Instruments.
20. M. H. Hassoun, *Fundamentals of Artificial Neural Networks* (MIT Press, Cambridge, MA, 1995).
21. J. Tien, T. D. Clark, D. Duffy, G. M. Whitesides, in preparation.
22. Y. Yin, B. Gates, Y. Xia, *Adv. Mater.*, in press.
23. R. R. A. Syms, *J. Microelectromech. Syst.* **8**, 448 (1999).
24. A. Ishikawa, U.S. Patent 6,069,682 (2000).
25. J. J. Hopfield and D. W. Tank, *Science* **233**, 625 (1986).
26. C. Mead, *Proc. IEEE* **78**, 1629 (1990).
27. P. D. Tougaw and C. S. Lent, *J. Appl. Phys.* **75**, 1818 (1994).
28. J. R. Heath, P. J. Kuekes, G. S. Snider, R. S. Williams, *Science* **280**, 1716 (1998).


29. Supported by Defense Advanced Research Projects Agency/SPAWAR/AFRL and the NSF (CHE-9901358 and ECS-9729405). We thank S. Brittain for help with photography.

21 April 2000; accepted 22 June 2000


# A [2]Catenane-Based Solid State Electronically Reconfigurable Switch


**Charles P. Collier, Gunter Mattersteig, Eric W. Wong, Yi Luo, Kristen Beverly, José Sampaio, Françisco M. Raymo, J. Fraser Stoddart,* James R. Heath***



**A solid state, electronically addressable, bistable [2]catenane-based molecular switching device was fabricated from a single monolayer of the [2]catenane, anchored with phospholipid counterions, and sandwiched between an n-type polycrystalline silicon bottom electrode and a metallic top electrode. The device exhibits hysteretic (bistable) current/voltage characteristics. The switch is opened at +2 volts, closed at −2 volts, and read at ~0.1 volt and may be recycled many times under ambient conditions. A mechanochemical mechanism for the action of the switch is presented and shown to be consistent with temperature-dependent measurements of the device operation.**


Modern molecular electronics began in 1974 when Aviram and Ratner (*1*) proposed a molecular rectifier based on an asymmetric molecular tunneling junction. As various synthetic and analytical tools have been developed, it has become possible to contemplate a real technology based on molecular electronic devices. Several fundamental devices using molecules have recently been demonstrated, including rectifiers (*2*), resonant tunnel junctions (*3*), and singly settable molecular switches that can be electronically configured for wired-logic gates (*4, 5*). In this report, we describe a reconfigurable molecular-based solid state switch capable of ambient operation. The device was fabricated from a single