Manycore Processor Networks with Monolithic Integrated CMOS Photonics

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Abstract: This paper presents an overview of advances in highly-integrated photonic networks for emerging manycore processors. It explores the tight interaction among logical and physical implementations of all-to-all core-to-core and core-to-DRAM networks, and underlying photonic devices.

OCIS codes: (200.4650) Optical interconnects; (250.5300) Photonic integrated circuits;

1. Introduction

Power-constrained process scaling is driving processor design towards increased levels of parallelism, with modern processors already at tens of cores on a single die [1,2] and projections of core count scaling into hundreds over the next decade. To keep scaling the performance, this increase in core count has to be followed by the corresponding increase in core-to-core and core-to-memory bandwidth. In addition to improving the core energy-efficiency, the big emerging problem is that electrical interconnect solutions (both on-chip and off-chip) cannot meet the increased bandwidth demand from growing number of cores. Due to pin-density, wire-bandwidth and power dissipation limits, the projected future enhancements of existing electrical DRAM interfaces, [3], are not expected to supply sufficient bandwidth with reasonable power consumption and packaging cost. Similar issues also limit energy-efficiency and bandwidth density of global on-chip wires [4]. To overcome this performance wall, an interconnect technology with both high energy-efficiency and bandwidth density is needed. With its potential for energy-efficient modulation and detection, and dense wavelength division multiplexing (DWDM), silicon-photonic interconnect technology is well suited to alleviate this bottleneck, however its application has to be carefully tailored to both the underlying process technology and the desired network topology.

2. Monolithic integration of CMOS photonics

Most initial efforts in silicon photonic interconnects have relied upon specialized processes, such as silicon-on-insulator (SOI) with several-micron thick buried oxide (BOX) [5], which are not compatible with processes used in processor fabrication. Apart from preserving the massive investment in standard fabrication technology, monolithic integration also reduces the area and energy costs of interfacing electrical and optical components and provides higher integrated bandwidth density. Recently developed infrastructure for photonic chip design and post-fabrication processing methodology [6,7] enabled for the first time a monolithic integration of polysilicon and silicon-based photonic devices in a standard bulk CMOS and thin BOX SOI fabrication flows commonly used for processors.

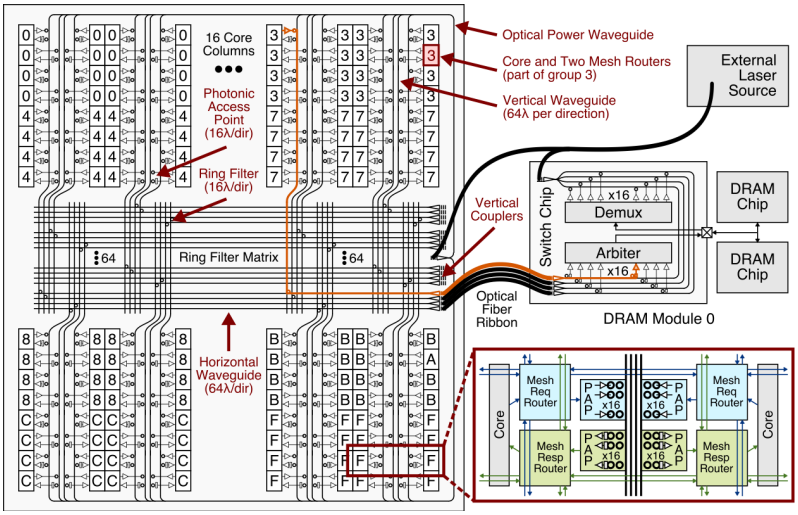

Fig. 1. A 256 core processor with a monolithic electro-optical core-to-DRAM shared memory network [8].

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Based on this technology and tight interaction between design of photonic interconnect components (waveguides, ring-resonators, modulators, photo-detectors, waveguide crossings), choice of network topology and implementation, in [8] we have proposed an efficient hybrid electro-optical core-to-DRAM shared memory network shown in Fig. 1, which provides a near ten-fold improvement in throughput compared to optimized electrical networks projected to 22 nm process node and a 256-core processor.

3. Interaction of network topology, implementation and critical device properties

Both the choice of logical network and its physical implementation have a large impact on network performance and cost. In addition to the performance impact at the application level, this choice involves balancing various loss components, such as ring-resonator losses, waveguide crossings and waveguide loss, to minimize the optical power, along with minimizing the electrical power through optimized temperature control, modulation and detection energy-efficiency. In Fig. 2, we illustrate several physical topologies for an all-to-all butterfly network among 16-core clusters on a 256-core die. These topologies, however, can have very different optical power requirements, that even scale differently with network capacity (mapped into number of waveguides, through rings per waveguide, waveguide crossings, etc). For example, the network in Fig. 2(a) will require between 0.4 and 33 W of optical power for the capacity range of 40 - 300 Tb/s (~ 8 - 60 Bytes/cycle/core), while those in Fig. 2(b) and (c) would require 1.4 - 11 W and 0.5 - 4 W, for same capacity range, respectively. The example losses are calculated based on optimized waveguide crossing designs with approx 0.05 dB/crossing [10], ring-resonator through loss of 0.0001 dB [9] and waveguide loss of 1 dB/cm, all very challenging photonic device specifications. These large variations in required optical power mandate careful co-design of optical network topology, implementation and underlying photonic devices. They also indicate that power requirements scale differently depending both on the network topology, network size and the required throughput.

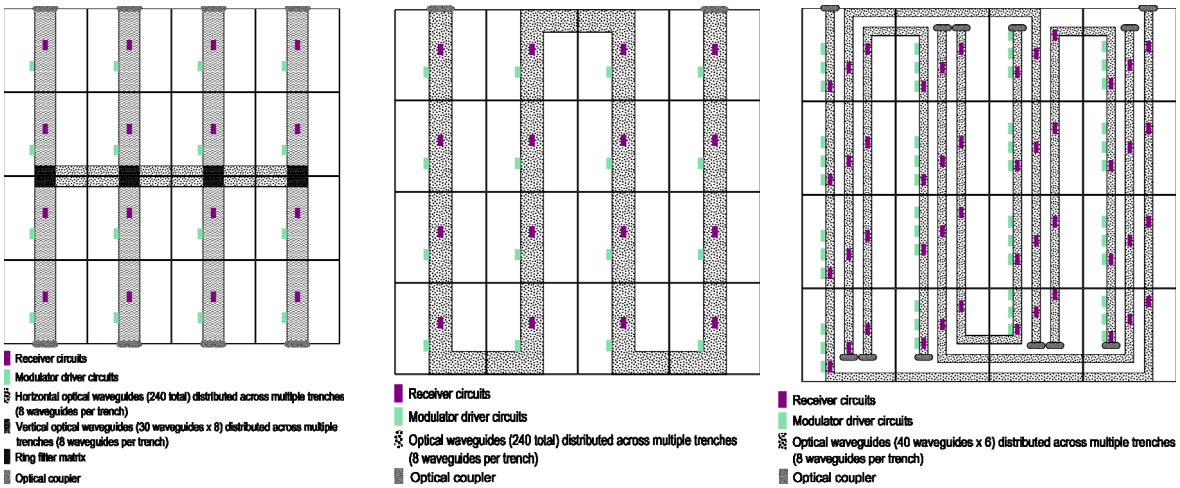

Fig. 2. Photonic network layouts for a butterfly network (a) ring-filter matrix [8], (b) serpentine, (c) loss-optimized

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