Influence of Metallic Tubes on the Reliability of CNTFET SRAMs: Error Mechanisms and Countermeasures

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ABSTRACT

Carbon nanotubes (CNTs) are considered as a possible successor to the CMOS technology. The adoption of these nanodevices for designing large VLSI systems, however, is limited by the unreliable manufacturing process. In this paper, we investigate the possibility of using CNTFETs to build SRAM arrays. We analyze the error mechanisms and show how stuck-at faults and pattern sensitive faults are caused by metallic tubes in different transistors of a 6-T SRAM cell. The results indicate the need of stronger error detecting codes than the widely used single-error-correcting, double-error-detecting codes in CMOS SRAMs.

Categories and Subject Descriptors

B.3.4 [**Memory Structures**]: Reliability, Testing, and Fault Tolerance—*Diagnostics*

General Terms

Reliability

Keywords

Reliability, CNTFET, SRAM

1. INTRODUCTION

The potential usage of carbon nanotube FETs (CNTFET) for the design of SRAM cells as an alternative to CMOS technologies has been investigated in the community. In [1], a multiple-V_T 6-T CNTFET SRAM cell based on dual-chirality selection of nano tubes was presented. In [2], the authors showed that compared to the CMOS SRAM cells, the CNTFET 6T SRAM cells have 84% less standby leakage power, 1.84 times of the speed, 21% larger static noise margin and are more resistant to temperature and channel length variations.

Although promising at first glance, the above works did not thoroughly analyze the influence of manufacturing variations of CNTFETs and the results are too optimistic. In practice, the adoption of CNTFET technology has been limited by the unreliable manufacturing process. Misaligned or mispositioned CNTs, metallic CNTs [3] and variations in dopings, diameters and densities of tubes due to the imperfect manufacturing process [4] result in high leakage power, delay, noise margin and even malfunction of transistors and logic error of the digital circuits. An initial estimation of the effects of the CNTFET imperfections described above on SRAM characteristics like the power consumption and the noise margin was presented in [5].

In this paper, we identify the possible error mechanisms caused by metallic tubes in CNTFET-based SRAM cells [1, 2] using detailed circuit level simulations and show how metallic tubes in the transistors of SRAM cells cause stuck-at faults and pattern sensitive faults. We estimate the bit error rate given the percentage of metallic tubes in a CNTFET. The results show that error control codes stronger than single-error-correcting, double-error-detecting codes used for CMOS SRAMS should be applied.

The rest of the paper is organized as follows. In Section 2, we briefly introduce the CNT technology and the main challenges in CNTFET manufacturing process. In Section 3, we analyze possible error mechanisms caused by metallic tubes in the SRAM cells.

2. CARBON NANOTUBE TECHNOLOGY

Carbon nanotube (CNT) technology has been proposed by various researchers as a potential successor to the CMOS technology due to its small dimension, large current carrying capacity and ballistic transport characteristic [6, 7]. CNTs can be used to build both transistors and wires as they can exhibit both semi-conducting and metallic behaviour. Circuits using CNTFETs have less standby leakage power, faster speed, larger static noise margin and are more resistant to temperature and channel length variations compared to circuits using the conventional CMOS transistors [2].

In spite of the potential advantages, the large-scale adoption of CNTFET technology has been limited by its unreliable manufacturing process. The limited control over the growth of CNTs may generate misaligned/mispositioned CNTs, which can cause incorrect functioning of the logic blocks [4]. The presence of metallic CNTs (33% for a typical growth process) can result in a short between the source and drain of the transistor, which will increase the leakage power, reduce the static noise margin and may cause delay variation and logic faults. Manufacturing variations in doping, diameters and densities of tubes directly influence the delay of the CNTFETs and may cause degraded noise margin and malfunctions of logic gates.

In this paper, we concentrate our analysis on the influence of metallic tubes in CNTFETs on the reliability of SRAM cells. The possible error mechanisms caused by metallic

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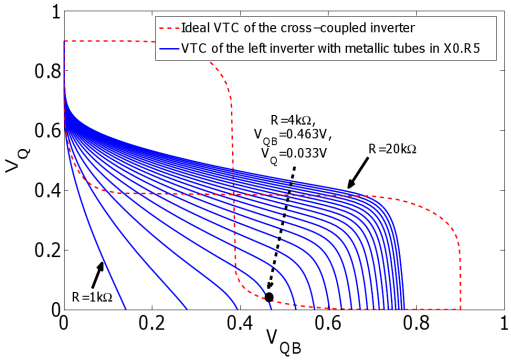

Figure 1: Influence of metallic tubes in pull down transistor on standby noise margin.

tubes in the transistors of SRAM cells are presented in the following section.

3. INFLUENCE OF METALLIC TUBES ON THE RELIABILITY OF SRAM CELLS

To analyze the effects of metallic tubes on the reliability of CNTFET SRAM cells, we conducted simulations in HSPICE based on Stanford CNTFET models [8]. We assume that the pitch (center-to-center distance of CNTs belonging to the same transistor) is 6 nm and the dielectric thickness is $3nm$. The supply voltage Vdd is $0.9V$. The chirality of all CNTs is selected to be $(19, 0)$ resulting in a tube diameter of 1.5 nm and a threshold voltage of 0.289 V [5]. The gate width $Wgate$ of the CNTFETs is $pitch \times \ \#\ tubes$. For all the other parameters, we use the default values provided by the Stanford CNTFET models.

In this work, the channel length of CNTFETs are 32 nm. The number of tubes for pull up transistors, access transistors and pull down transistors are assumed to be 8, 16 and 24 respectively. The pull-up ratio is 0.5. The pull-down ratio is 1.5. Both ratios are the same as shown in [1].

According to the measurement results shown in [9], we assume that the percentage of metallic CNTs p_m satisfies a normal distribution whose probability density function is $\frac{1}{\sqrt{2\pi\sigma^2}} e^{-(x-\mu)^2/(2\sigma^2)}$, where $\mu \approx 0.102$ is the mean and $\sigma \approx 0.0257$ is the standard deviation. We model each metallic tube as a resistor. The effective resistance of multiple metallic tubes is derived in the same way as for parallel resistors.

3.1 Stuck-at Faults

Metallic tubes in SRAM cells will introduce a short between its internal nodes and the bit line, the power supply or the ground depending on their locations. These shorts can cause stuck-at faults which result in read upsets or write failures. (For transistor names, please refer to Figure 2.)

3.1.1 Metallic tubes in the cross-coupled inverters

Let us assume there is a short between QB and Gnd introduced by metallic tubes in $M1$. As shown in Figure 1, the VTC of the inverter composed of $M1$ and $M2$ will move bottom left and the standby noise margin of the inverter will decrease as the effective resistance R of metallic tubes changes from $20k\Omega$ to $1k\Omega$. Because of the short between QB and Gnd, QB cannot be pulled up to Vdd when a 0 is stored in the cell (QB is high when a zero is stored). The stable state of V_{QB} can be derived from Figure 1 and is determined by the value of R. The existence of metallic

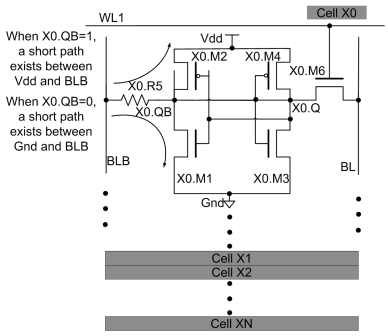

Figure 2: Multiple cells sharing the same bit lines in the SRAM array.

tubes in $M1$ may cause read upsets. Assume a logic 0 is stored in the cell (QB is high). When $R = 4k\Omega$, V_{QB} is only $0.463V$ (Figure 1) and a logic 1 will be mistakenly written in the cell after the word line WL is enabled during a read operation. When $R \leq 3k\Omega$, logic 0 cannot be written into the cell. Both of the cases will result in a stuck-at-1 fault ($V_Q = Vdd, V_{QB} = 0$).

REMARK 3.1. *The above simulation ignores the influence of the remaining semi-conducting tubes in $M1$ and the resulting transistor $M1'$ with a shrinked size. However, the effect of $M1'$ only shows up when V_Q is large enough to turn $M1'$ ON and will not improve the noise margin when a logic 0 is stored. The analysis of possible stuck-at-1 faults will still be valid if $M1'$ is considered. Similar analysis can be conducted for metallic tubes in $M2, M3$ and $M4$.*

3.1.2 Metallic tubes in the access transistors

Suppose a logic 0 is stored in the cell and there are metallic tubes in $M5$. Let R be the effective resistance of metallic tubes. Let $R_{M5'}$ be the ON resistance of $M5'$ composed of the remaining semi-conducting tubes in $M5$. Let R_A be the resistance between BLB and QB when the wordline is enabled, then $R_A = \frac{R_{M5'}R}{R_{M5'}+R} < R$. Assume a logic 1 is being written in the cell by setting $BLB = 0$ and $BL = Vdd$. Ideally, a reliable write is guaranteed by pulling QB below the threshold voltage of the transistor $M4$. However, when R_A is large, the effective pull-up ratio of the cell will increase. Simulation shows that when $R_A \geq 3k\Omega$, V_{QB} cannot be pulled low enough to ensure the writing of 1 in the cell, which results in a stuck-at-0 fault.

Possible stuck-at faults caused by metallic tubes in SRAM cells are summarized in Table 1. These errors can be detected by off-line testing methods, e.g. first write data into the memory and then verify it through read operations. For the case where more than one CNTFET contains metallic tubes, the overlay effect depends on the position, the number and the distribution of metallic tubes and can be derived using similar analysis.

3.2 Pattern-Sensitive Faults

SRAM cells belonging to the same column of the SRAM array share the same bit lines. Metallic tubes in the access transistors will introduce extra charging and discharging paths between the bitlines and the internal nodes of the SRAM cells and may affect the reading and writing operation on other cells in the same column (Figure 2).

3.2.1 Errors During Read Operations

Assume a logic 1 is stored in $X0$ ($X0.Q = Vdd, X0.QB = 0$) which contains metallic tubes (modeled as $X0.R5$) in the

Table 1: Stuck-at faults in SRAM cells caused by shorts introduced by metallic tubes

Position of metallic tubes	Initial state of QB	Final state of QB	Defects	Conditions
$M1$	-	-	Degraded noise margin	$R \geq 5k\Omega$
$M1$	1	0	Read upset (Stuck-at-1)	$R \approx 4k\Omega$
$M1$	0	0	Write failure (Stuck-at-1)	$R \leq 3k\Omega$
$M2$	-	-	Degraded noise margin	$R \geq 3k\Omega$
$M2$	1	1	Write failure (Stuck-at-0)	$R \leq 2k\Omega$
$M5$	1	1	Write failure (Stuck-at-0)	$R_A \geq 3k\Omega$

access transistor connecting BLB and $X0.QB$ and we try to read from another cell $X1$ in the same column storing a logic 0. To complete the read operation, BL and BLB will be precharged to Vdd and then the wordline of $X1$ will be enabled. Ideally, during the read operation BL will be discharged to 0 through $X1.M6$ and $X1.M3$ and BLB will maintain a voltage level close to Vdd given the fact that $X1.QB = Vdd$. Assume a basic differential sense amplifier [10] is used to generate the final output of the SRAM cell (Figure 3 (a)). When SAE is enabled, $SA.A$ will start discharging through $SA.M2$ and $SA.M4$.

Due to the short introduced by metallic tubes between BLB and $X0.QB$, BLB will be simultaneously charged through $X1.M2$ and $X1.M5$ and discharged through $X0.R5$ and $X0.M1$. As the resistance of $X0.R5$ becomes smaller, the stable voltage of BLB decreases and the ON resistance of $SA.M2$ becomes larger. The current I_D flowing through $SA.M2$ may be too small to discharge $SA.A$ fast enough to flip $SA.B$ and the output signal in the available time.

Assume the number of CNTs in each transistor of the sense amplifier is 16 and the clock period is 500 ps. The wordline of $X1$ and SAE are enabled for 300ps after BL and BLB are precharged to Vdd. The voltage curve of $SA.B$ for different values of $X0.R5$ is plotted in Figure 4. Simulation results show that when $X0.R5 \leq 0.8k\Omega$, the voltage of $SA.B$ cannot be charged high enough to pull down the output signal and a logic 1 is mistakenly read out from the cell.

Even worse, it is possible that the read operation on $X1$ will result in an un-wanted write of 1 in the same cell. Simulation results show that when $X0.R5 \leq 0.3k\Omega$, the voltage of $X1.QB$ can be pulled low enough through $X0.R5$ to flip the bit stored in the cross-coupled inverter. The error will stay until new contents are written in the cell.

Similar problems also exist for other types of sense amplifiers whose output converging speed depends on the absolute voltage difference between the two input signals. If more than one cell storing logic 1 contain metallic tubes in the access transistors connecting BLB and QB, as long as the effective resistance of all resistors introduced by metallic tubes in particular access transistors is less than a certain value (e.g. 0.8$k\Omega$ in our simulation), the failures described above will occur.

3.2.2 *Errors During Write Operations*

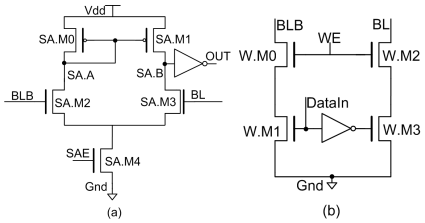

Figure 3: (a) Differential sense amplifier (b) Write driver

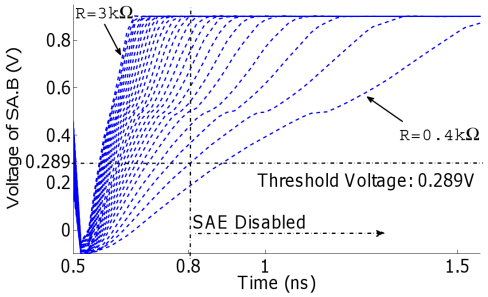

Figure 4: Voltage curve of $SA.B$ under the situations of different resistance of $X0.R5$.

Write 0 failure: Suppose $X0$ has metallic tubes in $M5$ and a logic 1 is stored in both $X0$ and $X1$ ($X0.QB = X1.QB = 0$). A 0 is being written in $X1$ by setting BLB to Vdd and BL to 0. Write failures are observed when $X0.R5 \leq 0.4k\Omega$, assuming a basic write driver is used [10] and each transistor in the write driver contains 48 CNTs (Figure 3 (b)). Ideally, the write operation is completed by pulling down $X1.Q$ to a voltage level lower than the threshold of $X1.M2$. However, due to the short introduced by the metallic tubes in $X1.M5$, $X1.QB$ will also be pulled down through the path $X1.M5 \rightarrow X0.R5 \rightarrow X0.M1$ when the wordline of $X1$ is enabled. As a result, $X1.Q$ cannot be pulled low enough to complete the write operation.

Write 1 failure: If both $X0$ and $X1$ store a logic 0 ($X0.QB = X1.QB = 1$) and a logic 1 is written in $X1$, $X1.QB$ will be pulled down through $W.M0$ and $W.M1$ in the write driver. Since $X0.QB = 1$, $X0.QB$ will pull up BLB as well as $X1.QB$ through $X0.R5$ introduced by the metallic tubes. When $1.4k\Omega \leq X0.R5 \leq 12k\Omega$, $X1.QB$ cannot be pulled low enough to ensure a writing of 1 in the cell. When $X0.R5 \leq 1.7k\Omega$, a 1 will be mistakenly written in $X0$.

Errors described in Section 3.2.1 and 3.2.2 are summarized in Table 2. These errors are pattern-sensitive and cannot be efficiently detected by off-line testing methods.

3.3 Estimation of the Probability of Errors in Memory Columns

In this section we estimate the probability for a column to have pattern-sensitive errors due to metallic tubes in the access transistors. To simplify the analysis, we only consider metallic tubes in the access transistors connecting BLB and QB. (A similar analysis can be performed for the case when there are also metallic tubes in access transistors connecting BL and Q.)

Let R_m be the resistance per metallic tube. To have a resistance no larger than 0.3$k\Omega$, at least $N_m = \frac{R_m}{0.3k}$ metallic tubes are required. Let N be the number of rows in the SRAM array. The total number of tubes in the access transistors connecting BLB and QB is $16N$ (each access transistor contains 16 tubes). Assume the percentage of metallic

Table 2: Pattern sensitive errors due to metallic tubes in $M5$ of $X0$

Operation*	$X0.QB$ (Initial)	$X1.QB$ (Initial)	$X0.QB$ (Final)	$X1.QB$ (Final)	Failures	Conditions
Read	0	1	0	1	Mis-read	$0.3k\Omega < X0.R5 \leq 0.8k\Omega$
Read	0	1	0	0	Mis-read, Un-wanted write in $X1$	$X0.R5 \leq 0.3k\Omega$
Write 0	0	0	0	0	Write Failure	$X0.R5 \leq 0.4k\Omega$
Write 1	1	1	1	1	Write Failure	$1.7k\Omega \leq X0.R5 \leq 12k\Omega$
Write 1	1	1	0	1	Write Failure, Un-wanted write in $X0$	$1.4k\Omega \leq X0.R5 \leq 1.7k\Omega$
Write 1	1	1	0	0	Un-wanted write in $X0$	$X0.R5 \leq 1.4k\Omega$

$*$: All the operations are on $X1$.

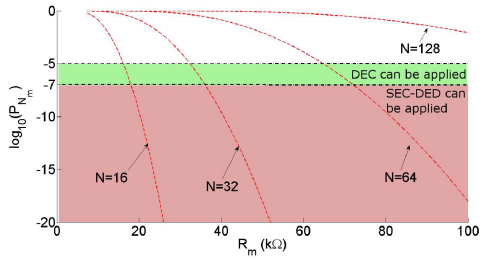

Figure 5: Column Failure Rate of SRAM Cells Due to Metallic Tubes in the Access Transistors.

tubes p_m satisfies a normal distribution with $\mu \approx 0.102$ and $\sigma \approx 0.0255$ [9] (Section 3). Let F_C be the complementary cumulative distribution function for the normal distribution. We have $F_C(x) = 0.5(1-erf(\frac{x-\mu}{\sqrt{2}\sigma}))$, where $erf(x)$ is the *error function*. The column may have pattern-sensitive errors if and only if the number of metallic tubes in all the access transistors connecting BLB and QB is at least N_m, which can be computed as $P_{N_m} = F_C(\frac{N_m}{16N}) = F_C(\frac{R_m}{N \cdot 4.8k})$. The probability that M columns have potential pattern-sensitive errors is $P_{N_m}^M$. Given the number of tubes per transistor, P_{N_m} is a function of the number of rows N and the resistance per metallic tube R_m. Generally speaking, larger N will increase the chance of having more than N_m metallic tubes in the access transistors. Smaller R_m will decrease the number of metallic tubes required to incur the mis-read or the write failure. Both cases will result in a worse P_{N_m} (Figure 5). Thereby, to increase the reliability of the SRAM, small N and large R_m should be targeted.

Table 3: Area overhead when protecting a 64-bit SRAM using different error correcting codes

Code	Number of Redundant bits	Percentage Overhead
SEC-DED	8	12.5%
DEC	14	21.9%
TEC	21	32.8%

Error correcting codes are widely used to correct errors in memory arrays. Figure 5 shows the regions where ECC with different error correcting capabilities are required to provide a satisfactory reliability for CNTFET SRAM arrays. When the bit error rate is smaller than 10^{-7}, the chance that the error is uncorrectable is less than 10^{-14} for systems protected by SEC-DED codes (e.g. linear extended Hamming [11]). If the bit error rate is larger than 10^{-7}, codes with higher error correcting capabilities are required (e.g. double-error-correcting (DEC) codes or triple-error-correcting (TEC) codes [11]). The area overhead of using ECC to protect memories is mainly determined by the number of extra cells needed to store the redundant bits of the ECC. As an example, we show the number of redundant bits and the corresponding overhead area of a SEC-DED code, a DEC code and a triple error correcting code (TEC) when protecting a 64-bit SRAM in Table 3.

One challenge of using linear codes with higher error correcting capabilities is in the design of the encoder and decoder. Compared to linear SEC-DED codes, the encoder and the decoder for linear multi-bit error correcting codes tend to have longer critical path because of the more complex encoding and decoding logic. Moreover, since the decoder for error correcting codes protecting CNTFET SRAMs is also built using unreliable technology, there is a need for the decoder itself to tolerate possible faults and errors.

4. CONCLUSIONS

We analyzed possible error mechanisms due to metallic tubes in the CNTFET SRAM cells. CNTFET SRAM array can have stuck-at faults or pattern-sensitive faults depending on the count and the positions of metallic tubes. Stuck-at faults can be detected using off-line testing methods. The errors from patten-sensitive faults are transient and their error rate is hard to predict due to the manufacturing variations (e.g. variations of the number of metallic tubes and the resistance per metallic tube). Multi-bit error correcting codes (DEC or TEC) will be required to provide a satisfactory reliability of CNTFET SRAMs.

5. REFERENCES

[1] S. Lin, Y.-B. Kim, and F. Lombardi, "Design of a cntfet-based sram cell by dual-chirality selection," *Nanotechnology, IEEE Transactions on*, vol. 9, no. 1, pp. 30 –37, jan. 2010.

[2] A. Kureshi and M. Hasan, "Performance comparison of cnfet- and cmos-based 6t sram cell in deep submicron," *Microelectronics Journal*, vol. 40, pp. 979 – 982, 2009.

[3] J. Zhang, N. P. Patil, and S. Mitra, "Design guidelines for metallic-carbon-nanotube-tolerant digital logic circuits," in *DATE '08*, pp. 1009–1014.

[4] N. Patil, J. Deng, A. Lin, H.-S. Wong, and S. Mitra, "Design methods for misaligned and mispositioned carbon-nanotube immune circuits," *CAD, IEEE Transactions on* , vol. 27, pp. 1725–1736, Oct. 2008.

[5] B. Ebrahimi and A. Afzali-Kusha, "Realistic cnfet based sram cell design for better write stability," july 2009, pp. 14 –18.

[6] N. Patil, J. Deng, S. Mitra, and H.-S. Wong, "Circuit-level performance benchmarking and scalability analysis of carbon nanotube transistor circuits," *Nanotechnology, IEEE Transactions on*, vol. 8, no. 1, pp. 37 –45, jan. 2009.

[7] A. H. Johnston, "Scaling and technology issues for soft error rates," ser. 4th Annual Research Conference on Reliability, 2000.

[8] http://nano.stanford.edu/models.php.

[9] Y. Li and etc, "Preferential growth of semiconducting single-walled carbon nanotubes by a plasma enhanced cvd method," *Nano Letters 2004 4 (2), 317-321.*

[10] *CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies*, 2008, ch. SRAM Circuit Design and Operation.

[11] F. MacWilliams and N. Sloane, *The Theory of Error-Correcting Codes*. NORTH-HOLLAND, 1983.