A Modeling and Exploration Framework for Interconnect Network Design in the Nanometer Era

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1. Introduction

To provide a well-balanced design in a power and area-constrained manycore system, and enable performance scaling with increase in number of cores, high-throughput energy-efficient on-chip networks need to be developed. We propose a design-space exploration framework to bridge technology, circuit, and architecture levels that will not only enable the evaluation of a new technology, but also the specification of the technology roadmap necessary to support the desired system roadmap.
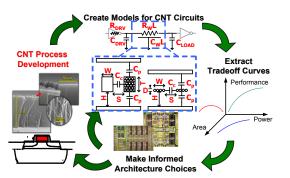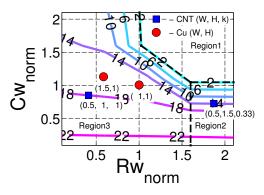
2. Integrated approach to interconnect network design

Figure 1: Integrated cyclic approach to explore CNT interconnect technology.

As we move into the nanometer regime, to explore new interconnect technologies, a generic and integrated approach, where interconnect designs are simultaneously optimized at all levels in the hierarchy is necessary. Figure 1 shows such an integrated approach that can be adopted for investigating the design space of carbon nanotube (CNT) interconnect technology. As a first step, circuit-level models are developed using the available CNT device models. Given today's dimensions of on-chip interconnects, and bandwidth density and area requirements, their inductance can be ignored and they can be modeled as RC interconnects. We explore the use of CNTs as both interconnects and vias. Various area, power and performance tradeoffs are explored at the circuit-level to map the RC design space using CNTs. These tradeoffs are then utilized to perform an architecture-level analysis using analytical models and detailed cycle-accurate simulations. The results obtained from the architectural analysis drive both circuit-level and device-level improvements needed to meet the overall system specifications. A similar approach can be easily adopted to study other interconnect technologies that can be mapped to the RC design space.

Figure 2: Ideal throughput (in Gbps) contour of a repeater-inserted cmesh network designed for a 64-node system, operating at 2.5 GHz, with 400 sq mm area and 10 W on-chip communication (wires and routers) power budget in 22 nm process for uniform random traffic. W = interconnect width, H = dielectric thickness, k = CNT non-ideality factor, Rw = resistance per unit length and Cw = capacitance per unit length.

3. Design example

As a design example, we consider a power-constrained concentrated mesh (cmesh) network for a 64-node system. Figure 2 shows the ideal network throughput contour plotted for the cmesh network for various combinations of Rw and Cw values, which have been normalized to the ITRS-predicted copper (Cu) interconnect for 22 nm technology. These Rw, Cw values correspond to various interconnect technologies (Cu and CNT) and dimensions. The RwCw design space is divided into three distinct regions that show the different effects of change in Rw and/or Cw on the ideal throughput. Using this throughput contour, design decisions could be made at all levels in the design hierarchy. For example, if an ideal throughput of 14 Gbps is desired for this 64-node system, then this cmesh network, with repeater-inserted interconnects designed using either of the four configurations in Figure 2 could be used as the underlying technology. However, if an ideal throughput of 18 Gbps is desired then only the CNT(0.5,1,1) configuration can be used.

4. Conclusion

As we approach serious scaling roadblocks in the next few process nodes, it is imperative to identify new emerging technologies that can complement or supplant CMOS in the future. We present an integrated cyclic approach to explore new interconnect technologies in the nanometer era for manycore systems, where on-chip interconnects are jointly optimized at all the levels in the design hierarchy to develop a complete interconnect solution – from interconnect technology to network topology.