Design and Optimization of Nonvolatile Multibit 1T1R Resistive RAM

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***Abstract*— Memristor-based random access memory (RAM) is being explored as a potential replacement for flash memory to sustain the historic trends in the improvement of density, access time, and energy consumption of nonvolatile memory. In this paper, we present the detailed functionality of multibit one-transistor one-memristor (1T1R) cell-based memory arrays, and propose circuit-level performance and energy models for an individual memory cell and the memory array as a whole. We consider titanium dioxide (TiO_2)- and hafnium oxide (HfO_x)-based memristors, and for these technologies, there is a sub-10% difference between energy and performance computed using our models and HSPICE simulations. Using a performance-driven design approach, the energy-optimized TiO_2-based resistive RAM (RRAM) array consumes the least write (4.06 pJ/b) and read energy (188 fJ/b) when storing 3 b/cell for 100-ns write and 1-ns read access times. Similarly, HfO_x-based RRAM array consumes the least write (365 fJ/b) and read energy (173 fJ/b) when storing 3 b/cell for 1-ns write and 200-ns read access times. We also present a detailed analysis of the implications of process, voltage, and temperature variations on the performance and energy consumption of a multibit RRAM cell.**

***Index Terms*— Memristor, modeling, reliability, resistive random access memory (RRAM).**

I. Introduction

CMOS technology scaling has been used to shrink device dimensions for density improvement, performance enhancement, and cost/bit reduction of flash memory arrays. However, it is becoming increasingly difficult to sustain this trend as individual CMOS devices are scaled into the nanometer regime [1]–[3]. Hence, there has been a significant push toward identifying and exploring alternate device technologies that can potentially supplant CMOS technology in future nonvolatile memory designs. Several emerging memory technologies including phase-change random access memory (PCRAM), magnetic RAM (MRAM), ferroelectric RAM (FeRAM), and resistive RAM (RRAM) are being explored as potential successors. Table I shows a head-to-head comparison of various nonvolatile emerging technologies with the conventional CMOS-based flash memories. Each technology has its pros and cons, which have made it difficult to identify a successor to CMOS technology. Among these technologies, PCRAM requires large energy for its resistive switching behavior, FeRAM suffers from signal degradation in scaling process, and MRAM has high endurance but it scales poorly and consumes large power because of large write currents. We focus on RRAM technology because of its simple structure, fast switching operation, and device scalability [4].

RRAM uses passive two-port memristors as storage elements. We present the design and optimization of low-power high-performance multibit one-transistor one-memristor (1T1R) RRAM arrays. The contributions of this paper are as follows.

1) We present the performance and energy models for n-bit 1T1R RRAM cell designed using titanium dioxide (TiO_2)- and hafnium oxide (HfO_x)-based memristors. These models consider the two-step read/write operation and the nonlinear behavior of TiO_2- and HfO_x-based memristors. These performance and energy models have been validated against HSPICE simulations (HSs). As a part of the modeling effort, we have also developed a SPICE model for HfO_x-based memristors.
2) We present a detailed discussion of the design and optimization of multibit 1T1R RRAM cells with TiO_2- and HfO_x-based memristors, and we calculate the optimum number of bits/cell considering energy and performance constraints of the entire multibit RRAM array.
3) We propose a mechanism for read reliability optimization in multibit RRAMs where the read noise margin is maximized using nonuniform memristor state assignment. We also compare the read energy consumption of multibit RRAM cells considering both nonuniform and conventional uniform memristor state assignments.
4) Using the performance and energy models, we present a detailed analysis of the impact of process (P), voltage (V), and temperature (T) variations on the access time, energy consumption, and reliability of multibit RRAM cells. We determine the optimum number of bits per 1T1R RRAM cell for both TiO_2- and HfO_x-based memristors that provides reliable operation under process, voltage, and temperature (PVT) variations.

In the rest of this paper, an overview of the memristor technology is presented in Section II. Section III discusses the related efforts in designing memristor-based circuits and systems. The detailed discussion of individual 1T1R n-bit memory cell and the overall architecture of a memory array are presented in Section IV. This is followed by the description of the performance models and energy models for read/write operation of the RRAM array, and the RRAM array's design

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TABLE I
COMPARISON BETWEEN FLASH MEMORY AND CURRENT EMERGING NONVOLATILE MEMORY TECHNOLOGIES

Memory type	Flash [5]	PCRAM [6]	MRAM [7]	FeRAM [8]	RRAM [9]
Cell	1T	1T1R	1T1R	1T1C	1T1R
R/W time (nsec)	60e3/2e6	76/20e3	12	200/134	8.5/10
R/W energy ($\frac{nJ}{bit}$)	-	15.3	0.9/1.3	9.77	-
Endurance	10^5	10^7	10^{16}	10^{13}	10^8
Retention	>10 yrs	>10 yrs	>10 yrs	>10 yrs	>10 yrs
Density ($\frac{Mb}{mm^2}$)	555	15.7	0.35	0.93	6.66
Tech. node (nm)	34	58	90	130	180

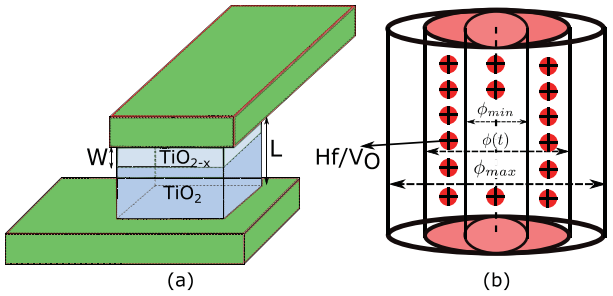

Fig. 1. Physical structure of (a) TiO_2-based memristor between two point contacts consisting of a highly conductive doped region and a highly resistive undoped region, where L is the thickness of the memristor and W is the thickness of the conductive region. (b) HfO_x-based memristor showing conductive filament (CF) growth/narrowing process where $\phi_{\min}$ and $\phi_{\max}$ are the minimum and maximum filament diameters, respectively.

and optimization in Section V. In Section VI, we explain the impact of PVT variations on the functionality of the multibit RRAM cells followed by concluding remarks in Section VII.

II. MEMRISTOR DEVICE TECHNOLOGY

Memristors provide a functional relationship between the charge and flux, which was first postulated in [10]. Several different implementations of memristors have been proposed in the literature. In this paper, we focus on TiO_2- and HfO_x-based memristor implementations. A detailed discussion of the alternate implementations of the memristors is presented in Section III.

The TiO_2-based memristor was first fabricated by Hewlett Packard [11]. The fabricated prototype had a highly resistive thin layer of TiO_2 and a second conductive deoxygenized TiO_{2-x} layer [Fig. 1(a)]. The change in the oxygen vacancies because of a voltage applied across the memristor modulated the dimension of the conductive region in the memristor. This resulted in a HRS and a LRS corresponding to the resistive and conductive regions of operation, respectively. We have summarized the equations required to model the TiO_2-based memristor functionality in Table II. The effective memristance of the memristor device can be calculated using (1) (proposed in [11]). Here, $x(t)$ is the state of the memristor [12] [calculated using (3)], $w(t)$ is the thickness of the conductive doped region as a function of time, and L is the memristor thickness.

The rate of change of the memristor state follows the ionic drift model, which is a function of the memristor physical parameters and the current through the memristor. As the current itself varies with time, the change of memristor state exhibits nonlinear behavior. This nonlinear behavior can be expressed using a window function shown in (5) [12]. In (5), $\mu_v \approx 3 \times 10^{-8} m^2/s/V$ [13] is the average dopant mobility and $F(x(t), p)$ is the window function, where the parameter p controls the memristor nonlinearity. Increasing p yields a flat window function for larger memristor states. Window functions that consider the linear ionic drift, and the nonlinear behavior that appears at the boundaries of the memristor state, have been proposed in [14] and [15]. Both these window functions, however, get stuck at the memristor state boundaries. We use the window function proposed in [16] for developing the performance and energy models of the TiO_2-based RRAM cell. This function models the nonlinear behavior of the rate of change of state without getting stuck at the boundaries and is given in (7). Here, sgn is a sign function that prevents the state of the cell from getting stuck at the borders.

In case of the HfO_x-based memristor, the set/reset (changing memristor resistance to $R_{\rm ON}/R_{\rm OFF}$) process is performed by increasing/decreasing the diameter of the CF using positively charged oxygen vacancies (V_O) or Hf ions migration in a thermally activated hopping process in the filament growth model [17]. Applying a voltage across the HfO_x-based memristor forces the positive ions to move along the direction of the electric field while increasing the maximum temperature along the CF and changing the effective cross-sectional diameter of the CF [Fig. 1(b)]. This rate of change of diameter was derived in [17] and is given by

$$\frac{d\phi}{dt} = Ae^{-\frac{E_{\rm A0}-\alpha q V}{kT_0\left(1+\frac{V^2}{8T_0\rho k_{\rm th}}\right)}} \tag{8}$$

where ϕ is the CF diameter, A is a pre-exponential constant, $E_{\rm A0}$ is the energy barrier for ion hopping, α is the barrier lowering coefficient, q is the elementary charge, V is the applied voltage across the memristor, k is the Boltzmann constant, T_0 is the room temperature, ρ is the electrical resistivity, and $k_{\rm th}$ is the thermal conductivity. A similar expression with a negative rate of change is used for modeling the reset process in HfO_x-based memristors. As voltage is applied across the HfO_x-based memristor, its cross-sectional area changes and the instantaneous resistance of the CF changes according to $R(t) = 4\rho L/\pi\phi(t)^2$. The rate of change of the diameter for HfO_x-based memristors in filament growth model for set and reset operations is shown in Fig. 2. The nominal parameter values of the memristor used for generating this plot are

TABLE II

EQUATIONS USED TO MODEL TiO_2- AND HfO_x-BASED MEMRISTORS. $x(t)$ IS THE NORMALIZED STATE OF THE MEMRISTOR, dx/dt IS THE RATE OF CHANGE OF STATE, AND $i(t)$ IS THE CURRENT THROUGH THE MEMRISTOR. $F(x(t), p)$ IS THE WINDOW FUNCTION, WHERE p IS THE CONTROL PARAMETER. R_{ON} AND R_{OFF} ARE THE MINIMUM AND MAXIMUM MEMRISTANCES [ALSO KNOWN AS LOW RESISTANCE STATE (LRS) AND HIGH RESISTANCE STATE (HRS)], RESPECTIVELY, AND $\beta = R_{OFF}/R_{ON}$

Parameter	TiO_2-based memristor	#	HfO_x-based memristor	#
Memristance	$M(t) = R_{ON}x(t) + R_{OFF}(1 - x(t))$	(1)	$M(t) = R_{ON}x(t) + R_{OFF}(1 - x(t))$	(2)
Memristor state	$x(t) = w(t)/L$	(3)	$x(t) = C\left(1 - \frac{\phi_{min}^2}{\phi(t)^2}\right), C = \frac{\phi_{max}^2}{\phi_{max}^2 - \phi_{min}^2} = 1 - 1/\beta$	(4)
Rate of change of state	$\frac{dx}{dt} = \frac{\mu_v R_{ON}}{L^2} i(t) F(x(t), p)$	(5)	$\frac{dx}{dt} = \frac{2C\sqrt{(1-x/C)^3}}{\phi_{min}} \frac{d\phi}{dt}$	(6)
Window function	$F(x(t), p) = 1 - (x - sgn(-i(t))^{2p}$	(7)	-	-

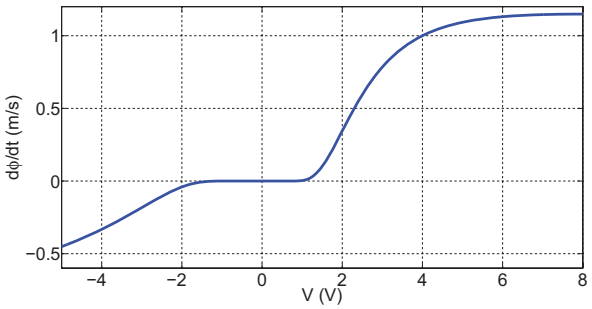

Fig. 2. Rate of diameter change for HfO_x-based memristors in a filament growth model [17] for set (V > 0) and reset (V < 0) operations as a function of voltage across the memristor.

TABLE III

PARAMETERS OF TiO_2-BASED [11] AND HfO_x-BASED [17], [9] MEMRISTORS USED FOR MODELING AND SIMULATIONS

Parameter	TiO_2	HfO_x
$R_{ON}(\Omega)$	100	3K
$R_{OFF}(\Omega)$	16K	10M
$L(nm)$	10	20
$E_{A0}(eV)$	-	1.2
$A(ms^{-1})$	-	1
α	-	0.3
$\rho(\mu\Omega cm)$	-	400
$k_{th}(Wm^{-1}K^{-1})$	-	20

```
.SUBCKT memristorHfOx PLUS MINUS phi
.PARAM phimin='sqrt(4*ro*L/(3.14*Roff))'
.PARAM phimax='sqrt(4*ro*L/(3.14*Ron))'
.PARAM C='phimax*phimax/(phimax*phimax-
phimin*phimin)'
Csv phi 0 1
.IC V(phi) 0.3
Emem PLUS AUX VOL='I(Emem)*(V(phi)*Ron+
(1-V(phi))*Roff)'
Rtest AUX MINUS 1
Gsv 0 phi
CUR='C*phimin*phimin*POW(sqrt(phimin*phimin
/(1-(phimax*phimax-phimin*phimin)*V(phi)/
(phimax*phimax))),-3)*2*A*exp(-1*(EA0-alpha*
q*V(PLUS,MINUS))/(k*T0*(1+POW(V(PLUS,MINUS)
,2)/(8*T0*ro*kth)))) * sgn(I(Emem)) *
sgn((1-V(phi)+
sgn(sgn(-I(Emem))+1))) * sgn((sgn(V(phi))+
sgn(I(Emem))+1))'
.ENDS memristorHfOx
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listed in Table III. To minimize the destruction of the stored data during read operation, we maintain the voltage across the memristor to be greater than −1.7 V. Similarly, during the write operation, we maintain the applied voltage between 1 and 4 V to minimize the set operation time.

To find the instantaneous memristance of the HfO_x RRAM, we define a new state function for HfO_x memristors in (4). Here, ϕ_{max} and ϕ_{min} are the maximum and minimum CF diameters corresponding to R_{ON} and R_{OFF}. This state function can be plugged into (1) to calculate the effective memristance. Considering the rate of change of the CF diameter in (1) and the state function in (4), we define the rate of change of the HfO_x-based memristor state in (6). The corresponding HSPICE netlist that we developed for HfO_x-based memristors is as follows:

The rate of change of the HfO_x-based memristor state is modeled as a voltage-controlled current source, and the combination of *sgn* functions guarantees the reliable set/reset operations, and the normalized memristor state does not get stuck when approaching one or zero.

III. RELATED WORK

Several oxide-based memristor devices have been proposed as storage elements in the design of RRAM arrays. HfO_x and TaO_x have been widely used as switching elements in RRAM cells [19]. Although several fabricated RRAM prototypes based on different switching materials have been reported in the literature, only a few reliable device models have been proposed for large-scale circuit-level simulations [17], [20]. A numerical model of filament growth based on thermally activated ion migration, which accounts for the resistance switching characteristics is proposed in [17]. This model (primarily developed for HfO_x-based 1T1R cell) matches the measurement results for different metal–oxide RRAM configurations (HfO_x/ZrO_x and NiO). The variation of switching parameters in RRAM devices using a trap-assisted

tunneling current solver considering the stochastic generation and recombination of oxygen vacancies is proposed in [21]. The compact model for the proposed RRAM switching behavior in [21] is introduced in [22], while the measurement results of the HfO_x-based prototypes verify this model in [23].

There are multiple efforts in place to develop accurate analytical model (AM) and SPICE model for the two-terminal memristor elements [17], [24], [25]. An analytical TiO_2 memristor model and the corresponding SPICE code that express both the static transport tunneling gap width and the dynamic behavior of the memristor state based on the measurement results are proposed in [24] and [26], respectively. In [27], a simplified yet accurate AM for the TiO_2 tunnel barrier phenomena analyzed in [24] with improved run times was developed. In [16], the authors developed a mathematical model for the prototype of memristor reported in [11] with dependent voltage and current sources as well as an auxiliary capacitor, which functions as an integrator to calculate the state of the memristor. In [28], a schematic diagram of the memristor SPICE macromodel based on a simplified window function for the rate of change of state was presented. A magnetic flux controlled SPICE model for memristors is proposed in [29] based on an exponential relationship for memristor I–V characteristics.

Several memory circuit/architecture topologies have been proposed in the literature based on the memristive structures. In [30], a Si-based memristive system to fabricate high-density crossbar arrays with high yield and OFF/ON ratio is used. A memristor-based TiO_2 memory cell is introduced in [31] and its functionality is evaluated using system-level simulations. An energy-efficient dual-element TiO_2-based memory structure is proposed in [32], in which each memory cell contains two memristors that store the complementary states. Similarly, a 2-b storage memristive cell is proposed in [33]. Both these multibit memory cells have large area. Content addressable memory designed using TiO_2 memristors has been introduced in [12]. A memristor-based lookup table design has been introduced in [34] to replace the static RAM (SRAM)-based field-programmable gate array (FPGA) design while achieving higher density. In [35], the functionality, performance, and power of several CMOS/memristor-based circuits with memory applications have been verified using a simulator based on a modified nodal analysis. An analysis of the peripheral circuitry of the crossbar array architecture is presented in [36]. A nonvolatile 8T2R SRAM cell that uses two HfO_x-based 1T1R cells along with the conventional 6T SRAM structure is introduced in [4] for low-power mobile applications. A bridge-like neural synaptic circuit with five TiO_2-based memristors, which is capable of performing sign/weight setting and synaptic multiplication operations, is introduced in [37]. In [38], the authors proposed adaptive write and read circuits for RRAM arrays to enhance yield and β ratio while eliminating large power consumption rising from the resistance fluctuations.

Memristors are highly vulnerable to process variation and several authors have analyzed its impact on the functionality of the memristive structures. Line-edge roughness (LERs) caused by uncertainties in the process of lithography and etching [39], oxide thickness fluctuations (OTFs) caused during sputtering or atomic layer deposition, and random discrete doping (RDDs), which leads to randomness in resistivity of the conductive as well as the resistive region of the memristor, are generally the main causes of process variations. In [40], the effect of cross-sectional area and oxide thickness variations on the memristor resistance was analyzed. In [41], the effect of LER and OTF on the state $x(t)$, the rate of change of state $dx(t)/dt$, and power dissipation variations of TiO_2-based memristor was analyzed. Using an error correcting code design for conventional dynamic RAM (DRAM) memory, the authors in [42] propose the detection and mitigation of errors rising from process variations in both MOS-based and crossbar memristive RRAM cells. In [43], a parallel–series reference cell scheme to decrease the reference current fluctuations in 1T1R RRAM structure was used. Moreover, using a process-temperature-aware dynamic bitline (BL) bias circuit, they lower the read disturbance caused by BL voltage variations.

IV. n-Bit 1T1R RRAM Cell Design and Array Architecture

In this section, we provide a detailed discussion for the functionality of an n-bit 1T1R RRAM cell followed by a description for the architecture of a memory array designed using this RRAM cell as the building block. We discuss the implementation of memory cells and arrays using both TiO_2- and HfO_x-based memristors.

A. RRAM Cell Design

The circuit of the 1T1R RRAM cell is similar to a DRAM cell and consists of an access transistor and a memristor as storage element. Similar to DRAM, the access transistor is enabled for both read and write operations. As the memristor device shows considerable nonlinearity when approaching the states of zero ($R_m = R_{\mathrm{OFF}}$) and one ($R_m = R_{\mathrm{ON}}$), it increases the required set/reset operation times at the two boundaries. We therefore ignore the states smaller than 0.1 and larger than 0.9 for faster set/reset, i.e., write operations. The n bits of a cell are stored in the 2^n distinct subranges in the range 0.1–0.9. For an n-bit cell design, the state assignment can be done such that maximum noise margin would be achieved. For example, for a 2-b RRAM cell, a memristor state below 0.3 corresponds to 00, a memristor state between 0.3 and 0.5 corresponds to 01, a memristor state between 0.5 and 0.7 corresponds to 11, and a memristor state above 0.7 corresponds to 10. We refer to this assignment as a uniform state assignment. A nonuniform state assignment could also be used for the n-bit cell. A comparison of the two assignments is presented in Section VI.

To perform the read operation, the loadline (LL) is driven to charge the BL through the memristor and access transistor. The read operation of the n-bit RRAM cell may be destructive and could require periodic refreshing of the cell data. For threshold-based memristor technologies, recent measurement results have shown that if the drive voltage is less than a threshold, the state does not change for fast read operations (Fig. 2). The TiO_2 RRAM—based on the ionic drift model—is not a threshold-based technology [27] and shows more

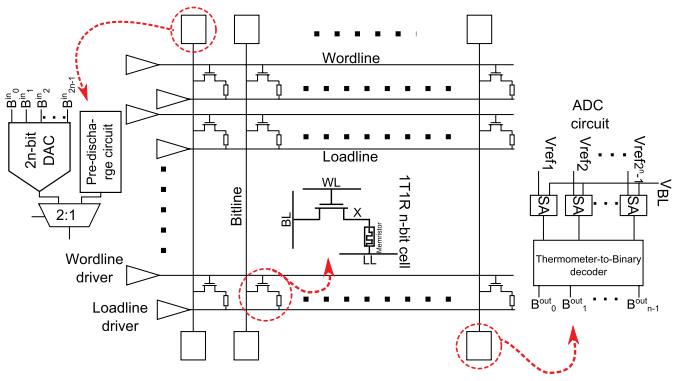

Fig. 3. n-bit/cell RRAM array architecture.

destructiveness during read cycles. A detailed analysis of the read destructiveness in multibit RRAM cells is proposed in Section V-A.

The write operation always consists of two suboperations—read followed by write as we need to know the data currently stored in the cell to determine the exact voltage that needs to be applied across the memristor to write new data. To perform the write operation, a positive or negative voltage is applied across the memristor for transitions to higher or lower states, respectively. The current flowing through the memristor changes the size of conductive region (in ionic drift model) or the diameter of the conductive filament (in filament growth model), thus increasing or decreasing the memristance. In the rest of this paper, we refer to the memory read and write operations as read_{top} and $\text{write}_{\text{top}}$, and the suboperations as read_{sub}, $\text{refresh}_{\text{sub}}$, and $\text{write}_{\text{sub}}$. Thus, $\text{read}_{\text{top}} = \text{read}_{\text{sub}} + \text{refresh}_{\text{sub}}$, whereas $\text{write}_{\text{top}} = \text{read}_{\text{sub}} + \text{write}_{\text{sub}}$.

B. RRAM Array Architecture

The overall architecture of a memory array built using 1T1R RRAM cells is similar to the conventional DRAM array, i.e., a wordline (WL) is used to select a row of cells, and a BL is shared by the cells in a column for reading/writing (Fig. 3). In a RRAM array architecture, to perform the read_{sub} operation, we first discharge the BL to 0 V, and then enable the WL and LL for a fixed predefined time. For the n-bit/cell array, when the WL and LL are enabled, the BL charges to one of the 2^n distinct voltages corresponding to the 2^n distinct data values (i.e., the memristor state) stored in the cell. For instance, in a 2-b/cell array, there will be four distinct data values. An analog-to-digital converter (ADC) can be used to retrieve n bits in each cell during the read operation. Each n-bit ADC consists of $2^n - 1$ differential sense amplifiers, each having the V_{BL} as one input and a unique reference voltage (V_{refi}) as the other input. For example, a 2-b/cell array needs three differential sense amplifiers. The $2^n - 1$ sense amplifiers are shared by all the cells in the column. The sense amplifiers could be shared between the columns to relax the area constraints on sense amplifier design. The rail-to-rail outputs of the sense amplifiers are fed to thermometer-to-binary code decoders that determine the exact data stored in the n-bit 1T1R cell and is given by bit B_0^{out}–$\text{B}_{\text{n}-1}^{\text{out}}$. For simulation and energy consumption analyses, we use the multiplexer-based decoder introduced in [44], which has a short critical path and consumes low power.

To perform the $\text{write}_{\text{sub}}$ operation, one of the $2^{2n} - 2^n$ different voltages (corresponding to the $2^n(2^n - 1)$ possible transitions for the n-bit RRAM cell) needs to be applied across the memristor. For example, a 2-b/cell array needs 12 V corresponding to 12 different transitions. The $\text{refresh}_{\text{sub}}$ operation would be similar to the $\text{write}_{\text{sub}}$ operation and the applied voltage will depend on the mechanism used for refresh operation. A $2n$-bit multiplexer-based digital-to-analog converter (DAC) can be used to generate the voltages to be applied across the memristor for $\text{write}_{\text{sub}}/\text{refresh}_{\text{sub}}$ operation. During $\text{write}_{\text{sub}}/\text{refresh}_{\text{sub}}$ operation, the outputs B_0^{out} and $\text{B}_{\text{n}-1}^{\text{out}}$ are connected to the B_0^{in} and $\text{B}_{\text{n}-1}^{\text{in}}$ inputs (corresponding to the current stored bits) and the data to be written into the cell are connected to the B_n^{in} and $\text{B}_{2\text{n}-1}^{\text{in}}$ inputs of the $2n$-bit DAC. This ensures the DAC generates the correct voltage to be applied to the BL for writing the data. For the 2-b/cell array, we need a 4-b DAC that generates 12 different set/reset voltages and an ADC with three sense amplifiers.

V. Performance and Energy Models for 1T1R RRAM Array

In this section, we discuss our performance and energy models for the n-bit 1T1R memory arrays designed using TiO_2- and HfO_x-based memristors. The parameters of TiO_2- and HfO_x-based memristors that are used in modeling and HSs are summarized in Table III.

A. Performance Models

As discussed in Section IV-A, the read_{top} and $\text{write}_{\text{top}}$ operations of the n-bit 1T1R cell consist of $\text{read}_{\text{sub}} + \text{refresh}_{\text{sub}}$ and $\text{read}_{\text{sub}} + \text{write}_{\text{sub}}$ operations, respectively. The equivalent circuit model for the 1T1R RRAM cell during read_{sub} operation is shown in Fig. 4. Here, R_m is the equivalent time-variant resistance of the memristor and R_{ch} is the access transistor channel resistance while operating in the triode region. The transmission gate, which is part of the predischarging path of the BL capacitor, is not included here as that transmission gate is switched OFF as soon as BL is discharged resulting in very high equivalent resistance for the transmission gate. C_{BL} and C_d are the BL capacitor and access transistor junction capacitor, respectively. In addition, R_{BL} is the total resistance of the BL. The BL voltage at the end of read_{sub} operation (i.e., after time T_R) will be

$$V_{\text{BL}} = V_{\text{LL}}\left(1 - e^{\frac{-T_R}{\left(R_m(t) + R_{\text{ch}} + 0.5R_{\text{BL}}\right)C_{\text{BL}}}}\right). \tag{9}$$

Here, the time constant of the junction capacitor (C_d) is much smaller than that of the BL capacitor (C_{BL}), and hence $C_{\text{BL}} + C_d$ has been approximated to be equal to C_{BL}. In addition, the term $0.5\,R_{\text{BL}}C_{\text{BL}}$ is the intrinsic time constant of the BL modeled as a distributed RC-line. We assume the BL, WL, and LL to be 1-mm long, each with total capacitance of 200 fF and total resistance of 6.5 kΩ corresponding to copper metal line with 50 nm × 50 nm cross-sectional area.

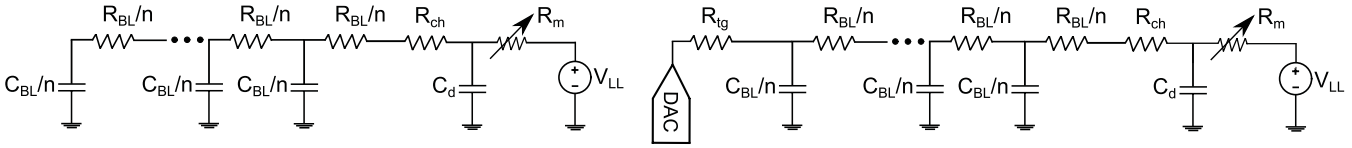

Fig. 4. Equivalent circuit of 1T1R cell for read_{sub} (left) and $\text{write}_{\text{sub}}/\text{refresh}_{\text{sub}}$ (right) operations.

TABLE IV

COMPARISON BETWEEN THE REFERENCE VOLTAGES DETERMINED USING AM AND HS FOR A READ_{sub} ACCESS TIME OF $T_R(\text{TiO}_2) = 1, 2$ ns AND $T_R(\text{HfO}_x) = 200, 400$ ns IN THE 2-B/CELL 1T1R RRAM. $V_{\text{LL}}(\text{TiO}_2) = 0.48$ V AND $V_{\text{LL}}(\text{HfO}_x) = 0.7$ V ARE CHOSEN TO REACH TO AT LEAST 25-mV DIFFERENCE BETWEEN THE TWO ADJACENT REFERENCE VOLTAGES. THE AVERAGE ERROR IS 5.7% FOR TiO_2 AND 0.151% FOR HfO_x

Reference Voltages	AM TiO_2 1 nsec	HS TiO_2 1 nsec	AM TiO_2 2 nsec	HS TiO_2 2 nsec	AM HfO_x 200 nsec	HS HfO_x 200 nsec	AM HfO_x 400 nsec	HS HfO_x 400 nsec
V_{ref1}	137.5 mV	120.5 mV	162 mV	158.17 mV	94.5 mV	94.79 mV	100.85 mV	100.84 mV
V_{ref2}	168 mV	153.5 mV	190.4 mV	188.69 mV	130.5 mV	130.9 mV	135.25 mV	135.23 mV
V_{ref3}	215.5 mV	202.5 mV	228.9 mV	231.37 mV	214 mV	214.6 mV	204.8 mV	204.81 mV

In addition, we assume the distributed RC-line model with 80 segments for all of the interconnects in the RRAM array architecture. As an example, for a 2-b RRAM cell, (9) can be used to define the three reference voltages (V_{ref1}, V_{ref2}, and V_{ref3}) to be the input to the three sense amplifiers that are used to differentiate between the four different stored values while performing read_{sub} operation. The BL voltage depends on the data stored in the memristor, i.e., the memristor state. For $V_{\text{ref1}} > V_{\text{BL}}$, $V_{\text{ref1}} < V_{\text{BL}} < V_{\text{ref2}}$, $V_{\text{ref2}} < V_{\text{BL}} < V_{\text{ref3}}$, and $V_{\text{ref3}} < V_{\text{BL}}$, the stored data is 00, 01, 11, and 10, respectively. We use Gray coding to increase the robustness and minimize the probability of getting 2-b error in the read operation. In Table IV, we compare the reference voltages calculated using the AM shown in (9) and using HS using 22-nm Predictive Technology Model [45]. Here, the read time of 1, 2 ns (for TiO_2) and 200, 400 ns (for HfO_x) is chosen based on the nominal β value for the two types of memristors in Table III. HfO_x has larger β and R_{OFF} values compared with TiO_2, and therefore, it needs higher read time for reliable read operation.

To ensure a reliable read operation, there should be sufficient difference in the four different voltages developed on the BL corresponding to the four different data that can be stored in the 2-b cell. For very large BL voltage development times, the BL can get completely charged to the LL voltage (V_{LL}). Simultaneously, for very small BL voltage development times, the difference in the BL voltages may not be large enough for the sense amplifier to correctly determine the data stored in the cell. The BL voltage of TiO_2- and HfO_x-based 2-b/cell RRAM cells for various BL voltage development times during read operation are shown in Figs. 5 and 6, respectively. For our 2-b/cell RRAM array example, we design our sense amplifier such that it needs at least 12.5-mV differential inputs. Hence, we need at least 25-mV difference between the adjacent BL voltages corresponding to the four different data that can be stored in the 2-b cell. The V_{ref} inputs to the three sense amplifiers are chosen based on BL voltages (corresponding to the four different data that can be stored in the cell) while ensuring the 12.5-mV differential input. From Figs. 5 and 6, we choose the minimum read access time that ensures 12.5-mV differential voltage at the sense amplifiers. Therefore, for the TiO_2- and HfO_x-based 2-b/cell RRAM cells, we choose 1 and 200 ns. In the TiO_2-based cell, for the 1-ns read access time, the four different BL voltages are 125, 150, 186, and 245 mV. The corresponding V_{ref1}, V_{ref2}, and V_{ref3} values are 137.5, 168, and 215.5 mV, respectively. Similarly, in the HfO_x-based cell, for the 200-ns read access time, the four different BL voltages are 82, 107, 154, and 274 mV. The corresponding V_{ref1}, V_{ref2}, and V_{ref3} values are 94.5, 130.5, and 214 mV, respectively. The read times as a function of number of bits/cell (n) is shown in Fig. 7. These read times have been chosen using the same approach as described above for the 2-b/cell RRAM cell. As the value of n increases, we need larger read times to ensure the reliable read operation.

As discussed in Section IV-A, the read_{sub} operation of the 1T1R cell can be destructive. The read destructiveness of TiO_2-based memristors is larger compared with HfO_x-based memristors for the same LL voltage (V_{LL}). The TiO_2-based memristor therefore needs to be refreshed more frequently than HfO_x-based memristor. Considering the rate of change of state for TiO_2 RRAM in (5), the number of consecutive read operations that will not destruct the stored data in multibit TiO_2-based 1T1R RRAM cell, i.e., the refresh threshold can be written as follows:

$$t_{\text{ref}-\text{TiO}_2} \approx \frac{(x_{\max} - x_{\min})(R_{\text{m(x)}} + R_{\text{ch}})}{2^n \gamma\, T_R V_{\text{LL}} (1 - (x-1)^{2p})}. \tag{10}$$

Here, $R_{\text{m(x)}}$ is the resistance of the memristor for each state, n is the number of bits/cell, T_R is the read access time, and $x_{\max}$ and $x_{\min}$ are the maximum and minimum normalized memristor states (0.9 and 0.1 in this paper), respectively, and $\gamma = \mu_v R_{\text{ON}}/L^2$. Large V_{LL}, n, and R_{ON} values (smaller β) necessitate more frequent refresh operation in the multibit RRAM cell. The contour plots of the number of consecutive nondestructive read operations in multibit TiO_2 RRAM is shown in Fig. 8 for different n (number of bits/cell) and V_{LL} values for a memristor with initial state of $x = 0.9$. In case of the highly destructive multibit TiO_2 memristor, we explored two different refresh schemes: a refresh operation

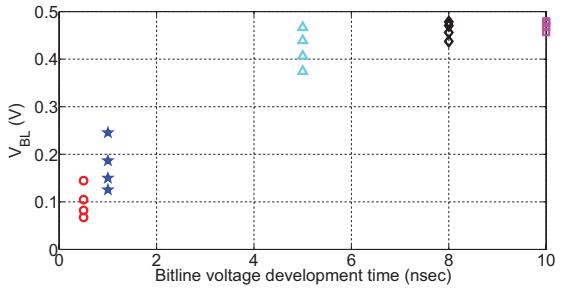

Fig. 5. BL voltage of a 2-b/cell TiO_2-based RRAM for different BL voltage development times.

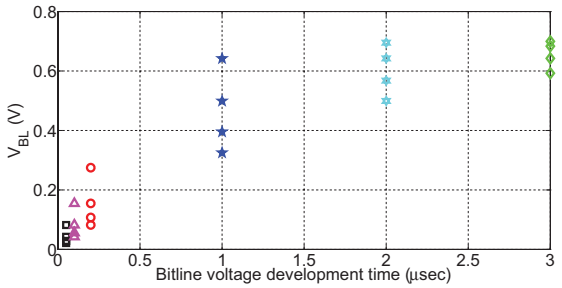

Fig. 6. BL voltage of a 2-b/cell HfO_x-based RRAM for different BL voltage development times.

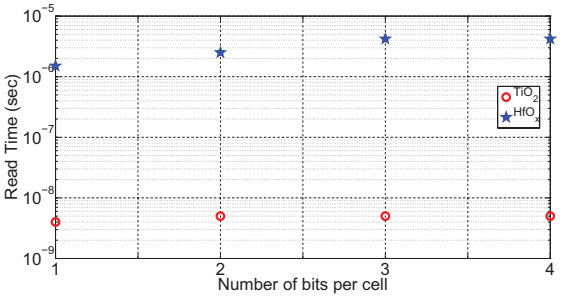

Fig. 7. Read time of a multibit RRAM cell for different number of bits/cell.

can be performed after each read cycle to compensate for destructiveness [40]. In this refresh scheme, we apply a $-V_{\rm LL}$ for the same duration as $\text{read}_{\rm sub}$. This doubles the read energy and lowers the performance of the RRAM array. A second refresh approach is to use a counter to track the current state of the memristor as well as the number of consecutive read operations. A refresh operation is done once the number of consecutive read operations on the multibit TiO_2 RRAM cell exceeds the threshold. For instance, in a 3-b/cell TiO_2-based RRAM array with $V_{\rm LL} = 0.1$ V, 50 consecutive read cycles will result in loss of data (Fig. 8), so a 6-b counter will be required to track the magnitude of destructiveness and perform refresh operation. Although the counter-based refresh approach seems more beneficial in multibit TiO_2 RRAM compared with the read followed by refresh scheme, our analysis shows that the energy and area overhead of the counter-based approach make it infeasible.

Considering the rate of change of state for HfO_x RRAM in (6), the number of consecutive nondestructive read operations in multibit HfO_x-based 1T1R RRAM cell will be

$$t_{\text{ref}-\text{HfO}_x} = \frac{\phi_{\min}(x_{\max} - x_{\min})}{2^{n+1} T_R C \sqrt{(1 - x/C)^3} \frac{d\phi}{dt}}. \tag{11}$$

The corresponding contour plots of the number of consecutive nondestructive read operations for different n and $V_{\rm LL}$ values for a memristor with initial state of $x = 0.9$ are shown in Fig. 8. The threshold-based CF growth mechanism in HfO_x memristor makes it more resilient to read destructiveness compared with ion drift mechanism-based TiO_2 memristors. As shown in Fig. 8, for small read voltage values, a large number of consecutive read operations are required to destruct the current state in multibit HfO_x RRAM technology. The refresh threshold proposed in (11) and shown in Fig. 8 exceeds the maximum allowed number of accesses (endurance) in the HfO_x-based RRAMs reported in [9] (Table I) and [4], which practically makes HfO_x as a nondestructive memristor technology at small read voltages. In case, large voltages are used for $\text{read}_{\rm sub}$ operation, then we might observe destructiveness of memristor state. To combat this, we propose to use a counter that tracks the current state of the memristor as well as the number of consecutive read operations. A refresh operation is done once the number of read operations exceeds the threshold given by (11). If we ignore the destructiveness (changing the memristance) during $\text{read}_{\rm sub}$ in the AM for simplicity, the resulting average error is 5.7% for TiO_2 and 0.151% for HfO_x.

The equivalent circuit model for the $\text{refresh}_{\rm sub}/\text{write}_{\rm sub}$ operation of a 1T1R RRAM cell is shown in Fig. 4. For the TiO_2-based memristor, the $\text{refresh}_{\rm sub}/\text{write}_{\rm sub}$ operation model uses the window function proposed in [16]. The switching time of the BL capacitor and the junction capacitor are the orders of magnitude lower than the switching time of the memristor. Hence, we do not consider these two capacitors in our AMs. Given the threshold voltage ($V_{\rm th}$) drop across the access transistor (i.e., $R_{\rm ch}$), the expression for memristor current during $\text{refresh}_{\rm sub}/\text{write}_{\rm sub}$ operation is as follows:

$$i_w(t) = \frac{V_{\rm BL} - V_{\rm th} - V_{\rm LL}}{R_m(t)}. \tag{12}$$

Using the window function in (7) and the rate of change of state in (12), the $\text{refresh}_{\rm sub}/\text{write}_{\rm sub}$ time can be approximated as

$$T_W = \frac{R_{\rm OFF} Q_i}{(V_{\rm BL} - V_{\rm LL} - V_{\rm th})\gamma} \tag{13}$$

where $\gamma = \mu_v R_{\rm ON}/L^2$. Here, $Q_i = \int_{x_i}^{x_{i+1}} 1 - x/1 - x^4\, dx$ is the nonlinear delay integral for transitions to higher memristor states, where x_i is the state of memristor and $Q_i = \int_{x_{i+1}}^{x_i} 1 - x/1 - (x-1)^4\, dx$ is the nonlinear delay integral for transitions to lower memristor states (note that here Q_i could be negative leading to a negative voltage across the memristor for transitions to lower states). Here, the resistance of the memristor is approximated as $R_m(t) \approx R_{\rm OFF}(1 - x(t))$ for simplicity. The integrals are determined from the window function we considered previously to model the nonlinearity of the memristor at the boundaries in (7) with $p = 2$. For the n-bit RRAM cell, the limits of the nonlinear delay integral Q_i will change based on 2^n different states. As an example, for the 2-b cell, we compared the required BL voltages for 12 possible $\text{write}_{\rm sub}$ transitions for 100- and 200-ns period in TiO_2-based 1T1R memory cells in Fig. 9. The $V_{\rm LL}$ voltage is maintained at 1.5 V for all the transitions. The average error between the

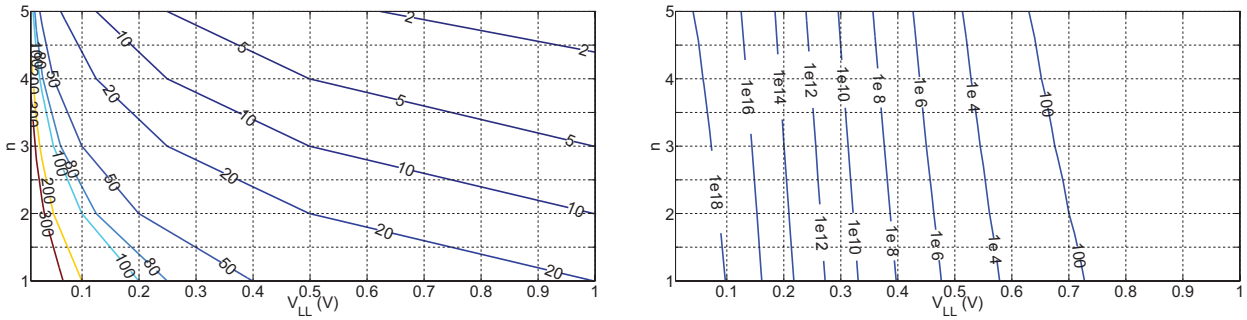

Fig. 8. Contour plots of the number of consecutive nondestructive read operations in multibit TiO_2-based (left) and HfO_x-based (right) RRAMs for different n and V_{LL} values ($x = 0.9$).

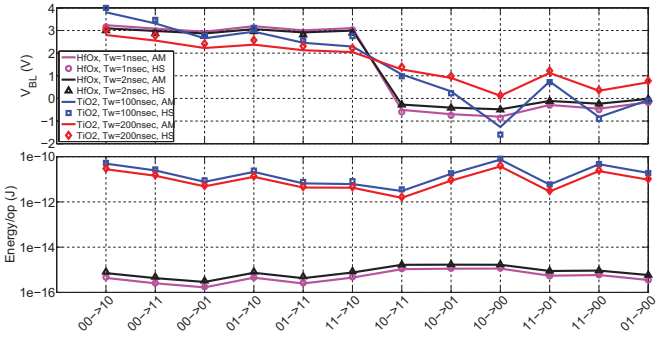

Fig. 9. Comparison between AM and HSs for BL voltage and energy dissipation in different TiO_2-based and HfO_x-based 2-b RRAM write/refresh operations. The V_{LL} voltage is 1.5 V for all the transitions. For BL voltage, the average error is 9.81% for TiO_2-based cell and 5.19% for HfO_x-based cell, whereas for energy dissipation, the average error is 8.71% for TiO_2-based cell and 5.25% for HfO_x-based cell.

AM and the HS results for a 2-b TiO_2-based 1T1R memory cell is 9.81%.

For the HfO_x-based memristor using the rate of change of state in (6), the set/reset time of the 1T1R RRAM cell can be modeled as

$$T_W = \frac{\phi_{\min}}{2C}\left(\frac{d\phi}{dt}\right)^{-1} U_i \tag{14}$$

where $U_i = \int_{x_i}^{x_{i+1}} dx/((1-x/C)^3)^{1/2}$ is the nonlinear delay integral for HfO_x-based memristors for transitions to higher states and $U_i = \int_{x_i+1}^{x_i} dx/((1-x/C)^3)^{1/2}$ is the nonlinear delay integral for HfO_x-based memristors for transitions to lower states. For the n-bit RRAM cell, the limits of the nonlinear delay integral U_i will change based on 2^n different states. Similar to the TiO_2-based memristor, there is a threshold voltage drop across the access transistor for set operation. The HfO_x cell write access time in (14) does not include the 0%–90% distributed RC-line transition time for BL ($R_{BL}C_{BL}$), which will later be included in the whole RRAM array design specification. Comparing results from the AM and the HS for 1- and 2-ns period for a 2-b HfO_x-based 1T1R memory cell in Fig. 9, the average error is 5.19%. The modeling error for HfO_x-based cell is different from the TiO_2-based cell because different electrical parameters were used for each type of cell, as summarized in Table III.

The contour plots for the set time constraints of 2-b/cell TiO_2-based and HfO_x-based RRAM are shown in Fig. 10. Write speed is limited by the voltage applied across the memristor (V_{mem}). The write operation of HfO_x-based memristor is faster compared with TiO_2-based because of the faster rate of change of state for HfO_x memristors.

B. Energy Models

In this section, we present the models for energy consumption during read_{sub} and $\text{write}_{\text{sub}}/\text{refresh}_{\text{sub}}$ operations. It should be noted that the energy consumed in the WL, BL, and LL depends on the aspect ratio of the memory array. Once the array structure is finalized, the energy can be determined based on BL capacitance (C_{BL}), LL capacitance (C_{LL}), and WL capacitance (C_{WL}). The energy dissipated in the cell during read_{sub} operation (for both TiO_2 and HfO_x) can be expressed as

$$E_R = \int_0^{T_R} V_{LL}\, i_R(t)\, dt \tag{15}$$

where $i_R(t)$ is the memristor current during the read_{sub} operation. Using the RC circuit model in Fig. 4, the energy dissipated in the n-bit RRAM cell at the end of read_{sub} operation will be

$$E_R = C_{BL} V_{LL}^2 \left(1 - e^{\frac{-T_R}{(R_m(t)+R_{ch}+0.5R_{BL})C_{BL}}}\right). \tag{16}$$

Table V compares the energy dissipation calculated from the AM and determined using HS during read_{sub} operation of a 2-b TiO_2-based RRAM cell having a latency of 1 ns as well as a 2-b HfO_x-based RRAM cell having a latency of 200 ns for different stored data values. The average error is 8.44% and 0.038% for TiO_2 and HfO_x, respectively.

The read energy contour plots for different number of bits/cell for both TiO_2- and HfO_x-based RRAMs are shown in Fig. 11. For each value of bits/cell and each read timing constraint, we find the V_{LL} value that gives at least 25-mV difference between two adjacent reference voltages of the sense amplifiers for reliable read operation. The difference between the reference voltages of the sense amplifiers is determined by the offset voltage of the input transistors in the voltage sense amplifiers and could be further reduced by increasing area at the expense of power [46]. Higher number of bits/cell requires larger drive voltages to increase read noise Margin, and therefore consumes more energy during read operation.

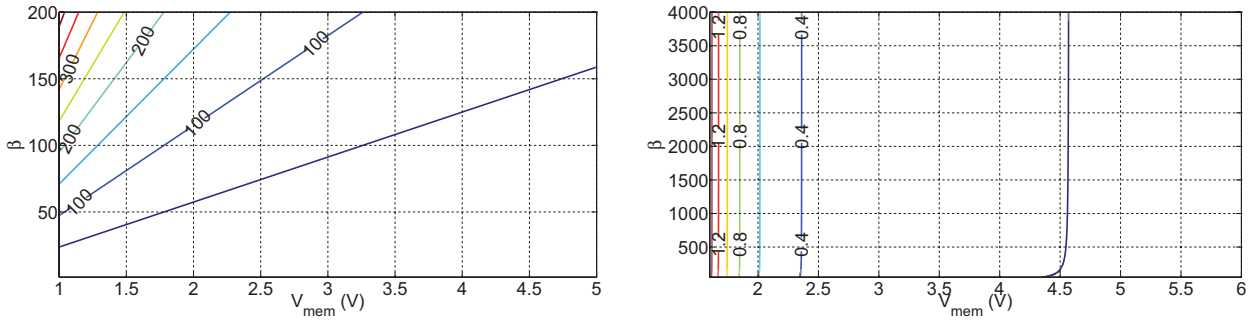

Fig. 10. Contour plots for set time (nanoseconds) in the 2-b/cell TiO_2-based (left) and HfO_x-based (right) RRAMs.

TABLE V
COMPARISON BETWEEN AM AND HS FOR ENERGY DISSIPATED IN THE CELL WHILE READING 2-B RRAM CELL WITH A READ ACCESS TIME OF $T_R(TiO_2) = 1$ ns AND $T_R(HfO_x) = 200$ ns. THE AVERAGE ERROR IS 8.44% AND 0.038% FOR TiO_2 AND HfO_x, RESPECTIVELY

Cell Data	AM TiO_2	HS TiO_2	AM HfO_x	HS HfO_x
00	12.03 fJ	12.84 fJ	11.51 fJ	11.50 fJ
01	14.40 fJ	15.58 fJ	15.03 fJ	15.02 fJ
11	17.91 fJ	19.68 fJ	21.65 fJ	21.65 fJ
10	23.57 fJ	26.48 fJ	38.47 fJ	38.47 fJ

Larger read times require lower drive voltages and dissipate lower amount of energy.

The instantaneous current of the memristor while performing $\text{refresh}_{\text{sub}}/\text{write}_{\text{sub}}$ operation in the TiO_2-based cell is determined by (12). Considering the V_{th} voltage drop across the access transistor, the energy dissipated in the cell during $\text{refresh}_{\text{sub}}/\text{write}_{\text{sub}}$ operation can be calculated as

$$E_W = \int_0^{T_W} (V_{\text{BL}} - V_{\text{th}} - V_{\text{LL}}) i_W(t)\, dt = \frac{(V_{\text{BL}} - V_{\text{th}} - V_{\text{LL}}) P_i}{\gamma} \tag{17}$$

where $\int i_W(t)dt = P_i/\gamma$ and $P_i = \int_{x_i}^{x_{i+1}} dx/1 - x^4$ is the nonlinear energy integral for transitions to higher memristor states and $P_i = \int_{x_{i+1}}^{x_i} dx/1 - (x-1)^4$ is the nonlinear energy integral for transitions to lower memristor states. The dissipated energy in the diffusion capacitor of the access transistor is ignored because it is much smaller than the overall cell energy. For the n-bit RRAM cell, the limits of the nonlinear energy integral P_i will change based on 2^n different states.

Fig. 9 compares the energy dissipated in a 2-b 1T1R cell for $\text{write}_{\text{sub}}$ in 12 possible transitions calculated using the AM and the HS for TiO_2-based configurations with transition time of $T_W = 100$ and 200 ns. The average error is 8.71%.

The $\text{write}_{\text{sub}}/\text{refresh}_{\text{sub}}$ energy in the HfO_x-based memristor is modeled as

$$E_W = \int_0^{T_W} V^2/R(t)\, dt \tag{18}$$

where V is the voltage across the memristor. Here, using $R(t) = (1 - x(t)/C)R_{\text{OFF}}$, the closed form expression for $\text{write}_{\text{sub}}/\text{refresh}_{\text{sub}}$ energy in n-bit 1T1R HfO_x-based cell is

$$E_W = \frac{V^2 \phi_{\min} \left(\frac{d\phi}{dt}\right)^{-1}}{2C R_{\text{OFF}}} S_i \tag{19}$$

where $S_i = \int_{x_i}^{x_{i+1}} dx/((1 - x/C)^5)^{1/2}$ is the nonlinear energy integral for HfO_x-based memristors. Because there is a threshold voltage drop across the access transistor, the write voltage (V) in (19) is chosen as one threshold voltage below the difference between V_{BL} and V_{LL} voltages. In the n-bit RRAM cell, the limits of the nonlinear energy integral S_i will change based on 2^n different states. The average error between the dissipated energy of a 2-b HfO_x RRAM cell model and the simulation results is 5.25% (Fig. 9). We do not consider the effect of subthreshold leakage in our energy analysis because all the transistors are working in strong inversion region of operation.

Using the energy models, we compare the different energy components of the 1T1R RRAM array for different number of bits/cell. The transition times of different components (other than the cell) in the RRAM array have been assumed constant for different number of bits and are 1.3 ns, 1.3 ns, 1 ns and 1 ns for wordline, loadline, ADC and Mux-based DAC, respectively. The energy consumption in different components of the RRAM array during read operation for TiO_2-based RRAMs is shown in Fig. 12. Cell energy increases during read operation for higher number of bits. This is due to higher LL voltages required for providing sufficient read noise margin for higher number of bits/cell. Because the read process of multibit TiO_2 RRAM is destructive (Fig. 8), we consider the energy of read, followed by a refresh operation in Fig. 12. The total WL energy is constant across all the cells. The number of sense amplifiers increases with number of bits/cell ($2^n - 1$ sense amplifiers for n-bit RRAM cell), and hence the energy/bit of the sense amplifiers increases. The same trend is observed for the decoder energy as the number of multiplexers increases with the number of bits/cell.

To increase the read reliability of multibit RRAM array, we assume there should be at least 25-mV difference between two adjacent reference voltages. One way to reach this voltage difference is to use uniform state assignment and increase the V_{LL} voltage. In the uniform state assignment scheme, there is a fixed distance between two adjacent states. Another way of reaching the 25-mV difference between two adjacent reference voltages is by lowering V_{LL} voltages, and choosing the appropriate memristor states such that the read reliability would be maximized. This approach is called nonuniform

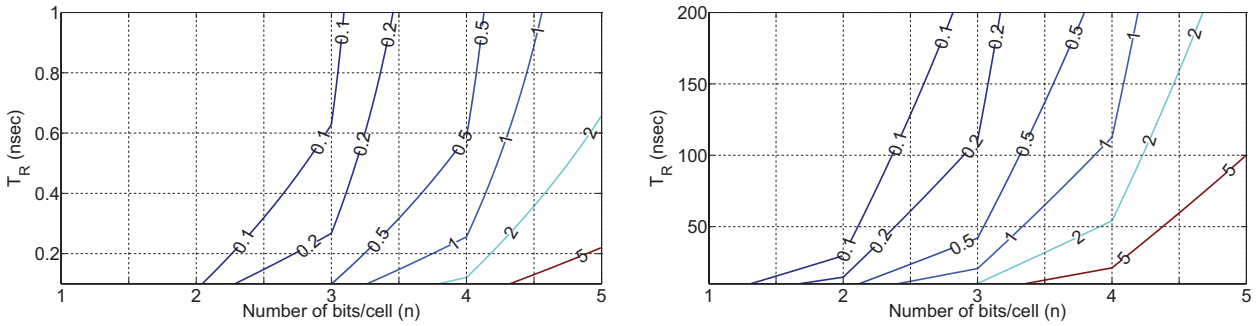

Fig. 11. Contour plots for average read energy (picojoules) in multibit TiO_2 RRAMs (left) and HfO_x RRAMs (right). We maintain at least 25-mV difference between adjacent reference voltages for reliable read operation.

state assignment where the 0.1–0.9 range for the state of a memristor is not uniformly shared between the 2^n different data that can be stored in the cell. Comparing uniform and nonuniform state assignment strategies, the nonuniform state assignment consumes lower energy because of lower V_{LL} values. The minimum total read energy/operation is consumed at $n = 2$ for uniform state assignment and $n = 3$ for nonuniform state assignment. Considering the same throughput constraint (# bits/cell $n = 3$) for both cases, nonuniform state assignment consumes 32.1% less energy than uniform state assignment.

Using the same approach, we show the energy consumption in different components of the RRAM array during read operation for HfO_x-based RRAMs using uniform and nonuniform state assignments in Fig. 12. The refresh energy of the multibit HfO_x memristor is amortized among different components of the array. Compared with TiO_2 and considering the same throughput constraint ($n = 3$), the total read energy consumption of the HfO_x RRAM array using nonuniform state assignment is 59.07% lower.

The energy consumed in various components of the RRAM array during the write operation for both TiO_2- and HfO_x-based RRAMs is shown in Fig. 13. Because the size of mux-based DAC increases with number of bits/RRAM cell, the energy consumption of the DAC increases accordingly. The total WL and LL energies are constant across all the cells. We determine the cell energy using the average energy value of all possible transitions for the n-bit cell. The TiO_2 cell energy dominates the energy dissipated in all the array components because of large set/reset time and lower resistance values for TiO_2 RRAM, while the HfO_x cell energy is much smaller than the energy in the remaining array components. The minimum total write energy/operation is consumed at $n = 3$ for both the cases.

VI. PVT Variation Analysis of n-Bit RRAM Cell

As shown in Section III, OTF and LER cause variations in memristor geometry [40], [41], [47] and RDD causes randomness in resistivity, which directly impacts the performance and energy dissipation of RRAM cells. In this section, we apply the Monte Carlo methodology [41] to our models for both TiO_2- and HfO_x-based memristors to analyze the influence of OTF, LER, and RDD on the performance and energy of the n-bit 1T1R RRAM cell. For our analysis, we exclude the variations in the energy and performance of the CMOS devices because of PVT variations to isolate and quantify the true impact of PVT variations on the memristors device functionality and the cell as a whole.

The LER of the memristor has been modeled as a combination of the low and high frequency domain disturbances in [41] and [48], and is given by

$$\text{LER} = L_{\text{LF}}.\sin(f_{\max}.r) + L_{\text{HF}}.z \tag{20}$$

where the sinusoid function with the amplitude of L_{LF} describes the low-frequency domain variations. Here, $f_{\max} = 1.8$ MHz is the mean of the low-frequency range with a uniform distribution represented as $r \in U(-1, 1)$. L_{HF} accounts for the high-frequency variations and z is considered to have a normal distribution function as $N(0, 1)$. The effect of OTF is usually modeled as a Gaussian distribution with a $\sigma = 2\%$ deviation from the nominal memristor thickness [40], [41]. In addition, RDD has been modeled as having a Gaussian distribution with $\sigma = 2\%$ [47] in the resistivity term in both ionic drift and filament growth models for TiO_2- and HfO_x-based RRAMs.

Considering the nominal parameters in Table III, we explore the effect of OTF, LER, and RDD on the states variations of both TiO_2- and HfO_x-based RRAMs. The state definition for ionic drift-based TiO_2 RRAM model is only a function for the ratio of the doped region to memristor thickness. The movement of dopants along the memristor thickness defines memristance [Fig. 1(a)]. Therefore, the state assignment will only be affected by OTF. In other words, LER and RDD will not change the state assignment of TiO_2-based RRAMs according to ionic drift memristor model. The impact of OTF on TiO_2-based RRAM with uniform and nonuniform state assignments for different number of stored bits ($1 \leq n \leq 4$) for 10 000 samples is shown in Fig. 14. The multibit TiO_2-based 1T1R RRAM cell is resilient to OTF-based process variations up to $n = 3$ for uniform state assignment and up to $n = 2$ for nonuniform state assignment, where no overlap is observed between the adjacent states.

The state definition for filament growth-based HfO_x RRAM model is only a function of filament diameter. Therefore, the state assignment will only be affected by LER. OTF and RDD will not change the state assignment of HfO_x-based RRAMs. The uniform and nonuniform state distributions of the HfO_x-based RRAM for different number of stored bits ($1 \leq n \leq 4$) are shown in Fig. 15. The multibit HfO_x-based 1T1R RRAM cell is resilient to LER-based process variations

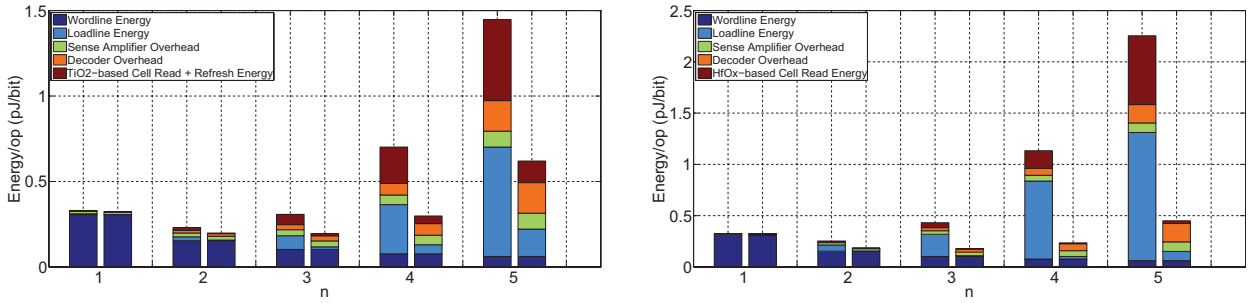

Fig. 12. Energy dissipated in different components of the multibit TiO_2-based ($T_R = 1$ ns) (left plot) and HfO_x-based ($T_R = 200$ ns) (right plot) RRAM array in read operation for uniform (left bar) and nonuniform (right bar) state assignments.

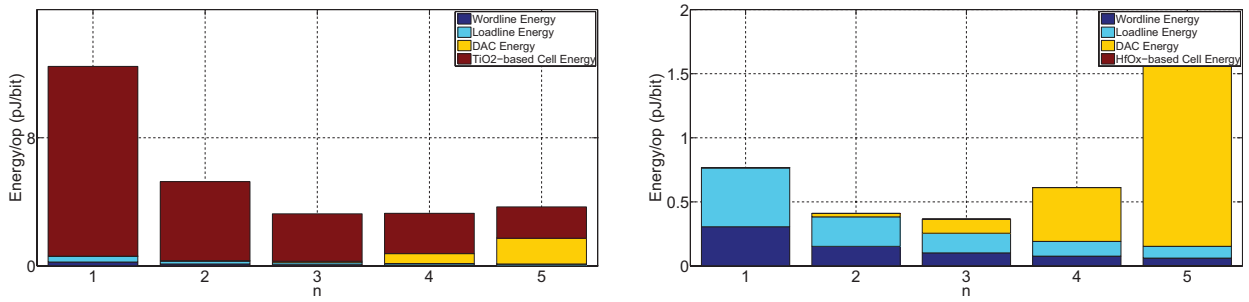

Fig. 13. Energy dissipated in different components of TiO_2-based ($T_W = 100$ ns) (left) and HfO_x-based ($T_W = 1$ ns) (right) RRAM array in write operation.

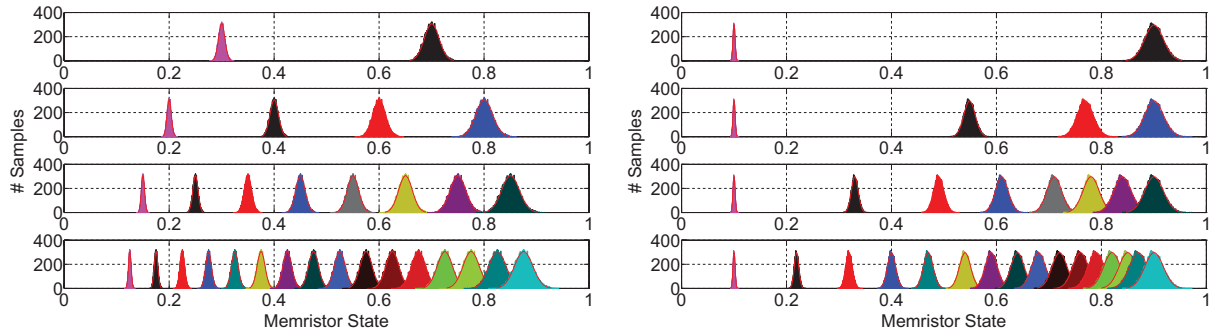

Fig. 14. Variations in the uniform state assignment (left) and nonuniform state assignment (right) of the multibit TiO_2-based memristor caused by OTF. The memristor state distribution for each number of bits/cell is such that the maximum process noise margin would be achieved.

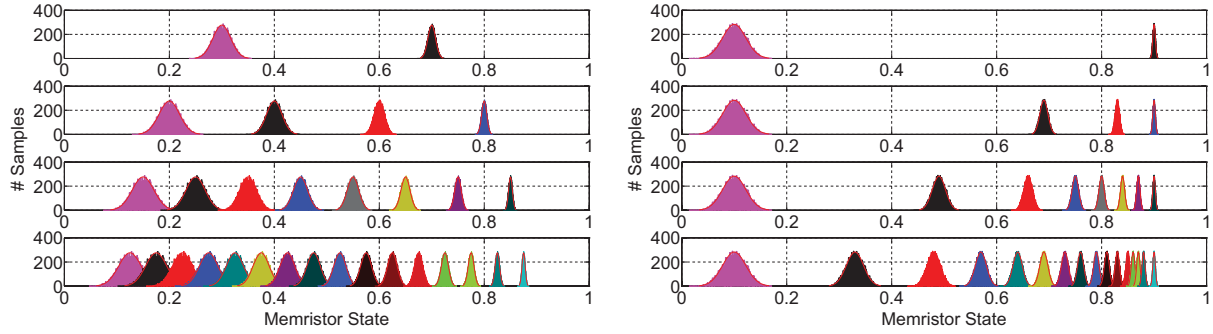

Fig. 15. Variations in the uniform state assignment (left) and nonuniform state assignment (right) of the multibit HfO_x-based memristor caused by LER. The memristor state distribution for each number of bits/cell is such that the maximum process noise margin would be achieved.

up to $n = 3$ where no overlap is observed between the adjacent states.

Table VI summarizes the effect of LER, OTF, and RDD on the state assignment, write time, write energy, read energy, and read destructiveness of the 3-b TiO_2- and HfO_x-based 1T1R cells. As discussed earlier, the TiO_2 memristor state is only affected by OTF, whereas the HfO_x memristor state is only affected by LER. The impact of LER, OTF, and RDD is quantified as $(3\sigma/\mu)\times 100\%$ value of each parameter. OTF has higher impact on the TiO_2 specifications compared with LER.

TABLE VI
$3\sigma/\mu$ OF THE 3-B TiO_2- AND HfO_x-BASED 1T1R CELL SPECIFICATION VARIATIONS BECAUSE OF LER, OTF, AND RDD. HERE, WT: WRITE TIME. WE: WRITE ENERGY. RE: READ ENERGY. RD: READ DESTRUCTIVENESS

Param.	LER TiO_2	OTF TiO_2	RDD TiO_2	LER HfO_x	OTF HfO_x	RDD HfO_x
$x(t)$	0%	6.01%	0%	12.58%	0%	0%
WT	0%	17.79%	8.52%	7.36%	0%	0.95%
WE	7.28%	12.03%	5.99%	21.96%	5.93%	5.03%
RE	3.78%	3.06%	3.01%	6.32%	5.34%	5.31%
RD	5.47%	7.50%	6.54%	3.65%	0%	63.25%

In addition, OTF has the highest impact on the write time variations for the multibit TiO_2 memristor because the TiO_2 set/reset time is a quadratic function of memristor thickness based on (13). Similarly, the effect of OTF on the write energy and read destructiveness of the TiO_2 RRAM is higher than LER. The variation in read destructiveness changes the refresh threshold, which affects the reliability of read operation. OTF and LER have similar impact on read energy because it is mostly dominated by BL variations according to (16). It should be noted that OTF has a minimal impact on the write time and read destructiveness of the HfO_x-based 1T1R cell as these two parameters are independent of the oxide thickness [see (13) and (14)]. LER has the highest impact on the write energy variations of the multibit HfO_x memristor because of its sensitivity to filament diameter fluctuations based on (19). The rate of change of diameter in the filament growth model has higher sensitivity to RDD at lower voltages. In other words, high set/reset voltages limit the effect of RDD in write time variations of HfO_x-based RRAMs. However, read destructiveness significantly changes with RDD because the applied read voltages are considerably low compared with write (set/reset) voltages, which deteriorates the read reliability of the HfO_x-based RRAMs.

The power supply noise in VLSI chips causes variations in the supply voltage applied to various transistors in a circuit, which in turn causes variations in performance and energy dissipation. Table VII summarizes the impact of voltage variations on write time, write energy, read energy, and read destructiveness of a 3-b RRAM cell. Without loss of generality, we explore two cases where each voltage reference has been assumed to have a Gaussian distribution with $3\sigma = 6\%$ and $3\sigma = 10\%$ of the nominal value. We calculate the write time and energy variations considering 56 possible transitions for the 3-b 1T1R RRAM cell. The write time and write energy of the HfO_x RRAM have more variations compared with TiO_2 because these two parameters are exponential functions of applied voltage in HfO_x RRAM according to (14) and (19). Comparing the rate of state change in (5) and (6), the destructiveness of the HfO_x-based memristor state is considerably more sensitive to voltage fluctuations. This will significantly affect the refresh threshold in (11) (Table VII). The read energy has similar amount of variations because of voltage fluctuations for both the materials according to (16).

We also analyzed the impact of temperature variations on performance and energy metrics of both TiO_2- and HfO_x-based memristors in the 3-b RRAM cell. The temperature dependency of the ionic drift model has been modeled in [49] where thermal resistance of the filament, defined as the ratio between the maximum temperature increase in the filament and the dissipated electrical power [50], for the state 1 ($R_{\rm ON}$) and state 0 ($R_{\rm OFF}$) in the TiO_2 filament are derived as follows:

$$R_{\rm th}(R_{\rm ON}) = L/(8k_M A_{\rm CF}). \quad (21)$$

$$R_{\rm th}(R_{\rm OFF}) \approx (2{\rm ArcSinh}[L/(\sqrt{A_{\rm CF}})] - 1.5)/(4k_I L). \quad (22)$$

Here, $k_M = 30$ W/mK and $k_I = 3$ W/mK [49] are the thermal conductances of the metal and insulator corresponding to titanium oxide thin films with oxygen vacancies conductive channels and $A_{\rm CF}$ is the filament area. The change in resistance of the RRAM based on ionic drift model follows $\Delta R_{R_{\rm OFF}, R_{\rm ON}} \propto \Delta T/(R_{\rm th} I^2)$, where I is the RRAM current.

TABLE VII
$3\sigma/\mu$ OF THE 3-B TiO_2- AND HfO_x-BASED 1T1R CELL SPECIFICATIONS BECAUSE OF VOLTAGE VARIATIONS FOR ($3\sigma_{V_{\rm ref}} = 6\%$) AND ($3\sigma_{V_{\rm ref}} = 10\%$)

Parameter	$3\sigma = 6\%$ TiO_2	$3\sigma = 10\%$ TiO_2	$3\sigma = 6\%$ HfO_x	$3\sigma = 10\%$ HfO_x
WT	5.92%	8.68%	8.10%	13.75%
WE	5.99%	9.01%	6.84%	11.55%
RE	12.08%	17.94%	11.92%	17.93%
RD	5.91%	9%	146.5%	229.98%

TABLE VIII
$3\sigma/\mu$ OF THE 3-B TiO_2- AND HfO_x-BASED 1T1R CELL SPECIFICATIONS BECAUSE OF TEMPERATURE VARIATIONS (ΔT)

Parameter	$\Delta T = 10$ TiO_2	$\Delta T = 30$ TiO_2	$\Delta T = 10$ HfO_x	$\Delta T = 30$ HfO_x
WT	4.47%	13.59%	7.56%	23.31%
WE	4.52%	13.75%	7.88%	23.40%
RE	0.07%	0.23%	24.79%	97.7%
RD @ $V_{LL} = 0.4V$	6.48%	19.22%	129.53%	427.75%

Table VIII summarizes the impact of temperature variations on write time, write energy, read energy, and destructiveness of both TiO_2- and HfO_x-based memristors in the 3-b RRAM cell. We explore two cases with nominal ambient temperature and variations of $\Delta T = 10$ K and $\Delta T = 30$ K. Temperature variations have a larger impact on the read destructiveness of the HfO_x-based memristor. The rate of change of diameter in HfO_x-based RRAMs because of temperature variations increases at lower applied voltages based on filament growth model in (8) [Fig. 16(a)]. The variations in write time and write energy of HfO_x RRAM is higher than TiO_2 because of the exponential temperature term in these metrics for HfO_x RRAM. The effect of temperature variation on the intermediate states of the multibit TiO_2 RRAM can be analyzed using the effective thermal resistance as $R_{\rm th} = R_{\rm th}(R_{\rm ON})||R_{\rm th}(R_{\rm OFF})$ [49], where the corresponding cross-sectional area for each state is plugged into the two thermal resistance expressions in (21) and (22). The effective thermal resistance of a 3-b TiO_2-based RRAM is shown in Fig. 16(b)

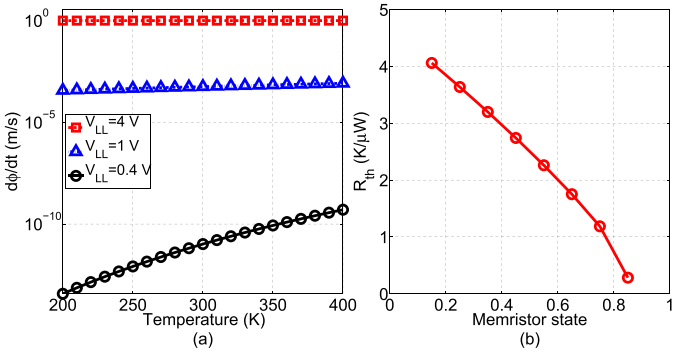

Fig. 16. (a) Diameter change of HfO_x-based memristors as a function of temperature for different applied voltages in filament growth model. Diameter shows higher variation with temperature at lower loadline voltages. (b) Effective thermal resistance of a 3-bit TiO_2-based RRAM as a function of memristor state.

for different memristor states. Temperature variations have minimal effect on the read energy fluctuations of TiO_2 RRAM because it is mostly affected by BL resistance (according to 9). This is, however, not the case for the HfO_x RRAM because its typical R_{OFF} value is the orders of magnitude larger than the BL resistance according to Table III. This will dominate the effect of temperature variations in HfO_x RRAM read energy fluctuations with respect to BL parasitic variations. The process, voltage, and temperature variation analysis for a cell can be further used to analyze the impact of variations on the overall RRAM array.

VII. Conclusion

In this paper, we presented the design and optimization of an n-bit 1T1R RRAM array designed using TiO_2- and HfO_x-based memristors. We first presented the models for the performance and energy of read and write operations in an n-bit 1T1R RRAM cells designed using TiO_2- and HfO_x-based memristors. A new SPICE netlist for HfO_x memristors was proposed based on the change in the CF diameter. We validated our performance and energy models against HSs, and the difference is less than 10% for both n-bit TiO_2- and HfO_x-based 1T1R cells. Using energy and performance constraints, we determined the optimum number of bits/cell in the multibit RRAM array to be three. The total write and read energy of the 3-b/cell TiO_2-based RRAM array was 4.06 and 188 fJ/b for 100 and 1 ns write and read access times, whereas the optimized 3-b/cell HfO_x-based RRAM array consumed 365 and 173 fJ/b for 1 and 200 ns write and read access times, respectively. We explored the tradeoff between the read energy consumption and the robustness against process variations for uniform and nonuniform memristor state assignments in the multibit RRAM array. Using the proposed models, we analyzed the effects of process, voltage, and temperature variations on performance and energy consumption and the reliability of n-bit 1T1R memory cells. Our analysis showed that multibit TiO_2 RRAM is more sensitive to OTF, whereas HfO_x RRAM is more sensitive to LER and is more susceptible to voltage and temperature variations.

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References

[1] K. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, Jul. 2012.
[2] S. Borkar, T. Karnik, and V. De, "Design and reliability challenges in nanometer technologies," in *Proc. 41st Annu. Design Autom. Conf.*, 2004, p. 75.
[3] C. T. Chuang, S. Mukhopadhyay, J. J. Kim, K. Kim, and R. Rao, "High-performance SRAM in nanoscale CMOS: Design challenges and techniques," in *Proc. IEEE Int. Workshop MTDT*, Dec. 2007, pp. 4–12.
[4] P.-F. Chiu, M.-F. Chang, C.-W. Wu, C.-H. Chuang, S.-S. Sheu, Y. S. Chen, and M.-J. Tsai, "Low store energy, low VDDmin, 8T2R nonvolatile latch and SRAM with vertical-stacked resistive memory (memristor) devices for low power mobile applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1483–1496, Jun. 2012.
[5] A. Macerola, A. D'Alessandro, A. Torsi, C. Cerafogli, C. Lattaro, C. Musilli, D. Rivers, E. Sirizotti, F. Paolini, G. Imondi, G. Naso, G. Santin, L. Botticchio, L. De Santis, L. Pilolli, M. L. Gallese, M. Incarnati, M. Tiburzi, P. Conenna, S. Perugini, V. Moschiano, W. Di Francesco, M. Goldman, C. Haid, D. Di Cicco, D. Orlandi, F. Rori, M. Rossini, T. Vali, R. Ghodsi, and F. Roohparvar, "A 3bit/cell 32 Gb NAND flash memory at 34 nm with 6 MB/s program throughput and with dynamic 2b/cell blocks configuration mode for a program throughput increase up to 13 MB/s," in *Proc. ISSCC*, Feb. 2010, pp. 444–445.
[6] H. Chung, B.-H. Jeong, B. J. Min, Y. don Choi, B.-H. Cho, J. Shin, J. Kim, J. Sunwoo, J. M. Park, Q. Wang, Y. J. Lee, S. Cha, D. Kwon, S. Kim, S. Kim, Y. Rho, M.-H. Park, J. Kim, I. Song, S. Jun, J. Lee, K. Kim, K. won Lim, W. R. Chung, C. Choi, H. Cho, I. Shin, W. Jun, S. Hwang, K.-W. Song, K. Lee, S. W. Chang, W.-Y. Cho, J.-H. Yoo, and Y.-H. Jun, "A 58nm 1.8V 1 Gb pram with 6.4MB/s program BW," in *Proc. IEEE ISSCC*, Feb. 2011, pp. 500–502.
[7] R. Nebashi, N. Sakimura, H. Honjo, S. Saito, Y. Ito, S. Miura, Y. Kato, K. Mori, Y. Ozaki, Y. Kobayashi, N. Ohshima, K. Kinoshita, T. Suzuki, K. Nagahara, N. Ishiwata, K. Suemitsu, S. Fukami, H. Hada, T. Sugibayashi, and N. Kasai, "A 90 nm 12 ns 32 Mb 2T1MTJ MRAM," in *Proc. IEEE ISSCC*, Feb. 2009, pp. 462–463.
[8] M. Qazi, M. Clinton, S. Bartling, and A. P. Chandrakasan, "A low-voltage 1 Mb feram in 0.13 μm CMOS featuring time-to-digital sensing for expanded operating margin in scaled CMOS," in *Proc. IEEE ISSCC*, Feb. 2011, pp. 208–210.
[9] P.-C. Chiang, W.-P. Lin, H.-Y. Lee, P.-S. Chen, Y.-S. Chen, T.-Y. Wu, F. T. Chen, K.-L. Su, M.-J. Kao, K.-H. Cheng, and M.-J. Tsai, "A 5 ns fast write multi-level non-volatile 1 K bits RRAM memory with advance write scheme," in *Proc. Symp. VLSI Circuits*, Jun. 2009, pp. 82–83.
[10] L. Chua, "Memristor—The missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.
[11] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.
[12] K. Eshraghian, K.-R. Cho, O. Kavehei, S.-K. Kang, D. Abbott, and S. M. Steve Kang "Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance search engines," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 8, pp. 1407–1417, Aug. 2011.
[13] K. Witrisal, "Memristor-based stored-reference receiver—The UWB solution," *Electron. Lett.*, vol. 45, no. 14, pp. 713–714, 2009.
[14] S. Benderli and T. A. Wey, "On SPICE macromodelling of TiO_2 memristors," *Electron. Lett.*, vol. 45, no. 7, pp. 377–379, 2009.
[15] Y. Joglekar and S. J. Wolf "The elusive memristor: Properties ofbasic electrical circuits," *Eur. J. Phys.*, vol. 30, no. 4, pp. 661–675, 2009.
[16] Z. Biolek, D. Biolek, and V. Biolkova, "SPICE model of memristor with nonlinear dopant drift," *Radioengineering*, vol. 18, no. 2, pp. 210–214, 2009.
[17] D. Ielmini, "Modeling the universal set/reset characteristics of bipolar RRAM by field- and temperature-driven filament growth," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4309–4317, Dec. 2011.
[18] Y. Chen, H. Y. Lee, P. S. Chen, P. Y. Gu, C. W. Chen, W. P. Lin, W. H. Liu, Y. Y. Hsu, S. S. Sheu, P.-C. Chiang, W. S. Chen, F.T. Chen, C. H. Lien, and M. J. Tsai, "Highly scalable hafnium oxide memory with improvements of resistive distribution and read disturb immunity," in *Proc. IEEE IEDM*, Dec. 2009, pp. 1–4.

[19] M. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y.-B. Kim, C.-J. Kim, D. H. Seo, S. Seo, U.-I. Chung, I.-K. Yoo, and K. Kim "A fast, high-endurance and scalable non-volatile memory device made from asymmetric Ta_2O_{5-x}/TaO_{2-x} bilayer structures," *Nat. Mater.*, vol. 10, pp. 625–630, Jan. 2011.

[20] G. Bersuker, D. C. Gilmer, D. Veksler, P. Kirsch, L. Vandelli, A. Padovani, L. Larcher, K. McKenna, A. Shluger, V. Iglesias, M. Porti, and M. Nafría, "Metal oxide resistive memory switching mechanism based on conductive filament properties," *J. Appl. Phys.*, vol. 110, no. 12, pp. 124518-1–124518-12, Dec. 2011.

[21] X. S. Guan, S. Yu, and H.-S. P. Wong, "On the switching parameter variation of metal-oxide RRAM—Part I: Physical modeling and simulation methodology," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1172–1182, Apr. 2012.

[22] X. S. Guan, S. Yu, and H.-S. P. Wong, "On the variability of HfO_x RRAM: From numerical simulation to compact modeling," in *Proc. Workshop Compact Model.*, 2012, pp. 815–820.

[23] S. Yu, G. Ximeng, and H.-S.P. Wong, "On the switching parameter variation of metal oxide RRAM—Part II: Model corroboration and device design strategy," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1183–1188, Apr. 2012.

[24] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching dynamics in titanium dioxide memristive devices," *J. Appl. Phys.*, vol. 106, no. 7, pp. 074508-1–074508-6, 2009.

[25] M. Zangeneh and A. Joshi, "Performance and energy models for memristor-based 1T1R RRAM cell," in *Proc. GLSVLSI*, 2012, pp. 9–14.

[26] H. Abdalla and M. D. Pickett, "SPICE modeling of memristors," in *Proc. IEEE ISCAS*, May 2011, pp. 1832–1835.

[27] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: Threshold adaptive memristor model," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 1, pp. 211–221, Jan. 2013.

[28] A. Rak and G. Cserey, "Macromodeling of the memristor in SPICE," *IEEE Trans. Comput. Aided Design Integr. Circuits Syst.*, vol. 29, no. 4, pp. 632–636, Apr. 2010.

[29] D. Batas and H. Fiedler, "A memristor SPICE implementation and a new approach for magnetic flux-controlled memristor modeling," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 250–255, Mar. 2011.

[30] S. H. Jo, K.-H. Kim, and W. Lu, "High-density crossbar arrays based on a Si memristive system," *Nano Lett.*, vol. 9, no. 2, pp. 870–874, 2009.

[31] Y. Ho, G. M. Huang, and P. Li, "Dynamical properties and design analysis for nonvolatile memristor memories," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 4, pp. 724–736, Apr. 2011.

[32] D. Niu, Y. Chen, and Y. Xie, "Low-power dual-element memristor based memory design," in *Proc. 16th ACM/IEEE ISLPED*, Aug. 2010, pp. 25–30.

[33] H. Manem and G. S. Rose, "A read-monitored write circuit for 1T1M multi-level memristor memories," in *Proc. ISCAS*, May 2011, pp. 2938–2941.

[34] Y.-C. Chen, W. Zhang, and H. Li, "A look up table design with 3D bipolar RRAMs," in *Proc. 17th ASP-DAC*, 2012, pp. 73–78.

[35] W. Fei, H. Yu, W. Zhang, and K. S. Yeo "Design exploration of hybrid CMOS and memristor circuit by new modified nodal analysis," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 6, pp. 1012–1025, Jun. 2012.

[36] C. Xu, X. Dong, N. P. Jouppi, and Y. Xie, "Design implications of memristor-based RRAM cross-point structures," in *Proc. DATE*, Mar. 2011, pp. 1–6.

[37] H. Kim, M. P. Sah, C. Yang, T. Roska, and L. O. Chua, "Neural synaptic weighting with a pulse-based memristor circuit," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 148–158, Jan. 2012.

[38] X. Xue, W. X. Jian, J. G. Yang, F. J. Xiao, G. Chen, X. L. Xu, Y. F. Xie, Y. Y. Lin, R. Huang, Q. T. Zhou, and J. G. Wu, "A 0.13 μm 8 Mb logic based CuxSiyO resistive memory with self-adaptive yield enhancement and operation power reduction," in *Proc. Symp. VLSI Circuits*, Jun. 2012, pp. 42–43.

[39] Z. Jiang, F. Zhao, W. Jing, P. D. Prewett, and K. Jiang, "Characterization of line edge roughness and line width roughness of nano-scale typical structures," in *Proc. 4th IEEE NEMS*, Jan. 2009, pp. 299–303.

[40] D. Niu, Y. Chen, C. Xu, and Y. Xie, "Impact of process variations on emerging memristor," in *Proc. 47th ACM/IEEE DAC*, Jun. 2010, pp. 877–882.

[41] M. Hu, H. Li, Y. Chen, X. Wang, and R. E. Pino, "Geometry variations analysis of TiO_2 thin-film and spintronic memristors," in *Proc. 16th ASP-DAC*, 2011, pp. 25–30.

[42] D. Niu, Y. Xiao, and Y. Xie, "Low power memristor-based ReRAM design with error correcting code," in *Proc. ASP-DAC*, 2012, pp. 79–84.

[43] S.-S. Sheu, M.-F. Chang, K.-F. Lin, C.-W. Wu, Y.-S. Chen, P.-F. Chiu, C.-C. Kuo, Y.-S. Yang, P.-C. Chiang, W.-P. Lin, C.-H. Lin, H.-Y. Lee, P.-Y. Gu, S.-M. Wang, F.T. Cen, K.-L. Su, C.-H. Lien, K.-H. Cheng, H.-T. Wu, T.-K. Ku, M.-J. Kao, and M.-J. Tsai "A 4 Mb embedded SLC resistive-RAM macro with 7.2 ns read-write random-access time and 160ns MLC-access capability," in *Proc. ISSCC*, 2011, pp. 200–202.

[44] E. Sail and M. Vesterbacka, "A multiplexer based decoder for flash analog-to-digital converters," in *Proc. TENCON*, vol. 4. Nov. 2004, pp. 250–253.

[45] (2011). *Predictive Technology Model (PTM)* [Online]. Available: http://ptm.asu.edu/

[46] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18 ps setup+hold time," in *Proc. IEEE ISSCC*, Feb. 2007, pp. 314–605.

[47] M. Hu, H. Li, and R. E. Pino, "Fast statistical model of TiO_2 thin-film memristor and design implication," in *Proc. IEEE/ACM ICCAD*, Nov. 2011, pp. 345–352.

[48] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic memristor through spin-torque-induced magnetization motion," *IEEE Elecron Device Lett.*, vol. 30, no. 3, pp. 294–297, Mar. 2009.

[49] D. Strukov and R. Williams, "Intrinsic constrains on thermally-assisted memristive switching," *Appl. Phys. A, Mater. Sci. Process.*, vol. 102, no. 4, pp. 851–855, 2011.

[50] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Filament conduction and reset mechanism in NiO-based resistive-switching memory (RRAM) devices," *IEEE Trans. Electron Devices*, vol. 56, no. 2, pp. 186–192, Feb. 2009.

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