Design and Optimization of Nonvolatile Multibit 1T1R Resistive RAM

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Abstract—Memristor-based random access memory (RAM) is being explored as a potential replacement for flash memory to sustain the historic trends in the improvement of density, access time, and energy consumption of nonvolatile memory. In this paper, we present the detailed functionality of multibit one-transistor one-memristor (1T1R) cell-based memory arrays, and propose circuit-level performance and energy models for an individual memory cell and the memory array as a whole. We consider titanium dioxide (TiO$_2$)- and hafnium oxide (HfO$_2$)-based memristors, and for these technologies, there is a sub-10% difference between energy and performance computed using our models and HSPICE simulations. Using a performance-driven design approach, the energy-optimized TiO$_2$-based resistive RAM (RRAM) array consumes the least write (4.06 pJ/b) and read energy (188 fJ/b) when storing 3 b/cell for 100-ns write and 1-ns read access times. Similarly, HfO$_2$-based RRAM array consumes the least write (365 fJ/b) and read energy (173 fJ/b) when storing 3 b/cell for 1-ns write and 200-ns read access times. We also present a detailed analysis of the implications of process, voltage, and temperature variations on the performance and energy consumption of a multibit RRAM cell.

Index Terms—Memristor, modeling, reliability, resistive random access memory (RRAM).

I. INTRODUCTION

CMOS technology scaling has been used to shrink device dimensions for density improvement, performance enhancement, and cost/bit reduction of flash memory arrays. However, it is becoming increasingly difficult to sustain this trend as individual CMOS devices are scaled into the nanometer regime [1]–[3]. Hence, there has been a significant push toward identifying and exploring alternate device technologies that can potentially supplant CMOS technology in future nonvolatile memory designs. Several emerging memory technologies including phase-change random access memory (PCRAM), magnetic RAM (MRAM), ferroelectric RAM (FeRAM), and resistive RAM (RRAM) are being explored as potential successors. Table I shows a head-to-head comparison of various nonvolatile emerging technologies with the conventional CMOS-based flash memories. Each technology has its pros and cons, which have made it difficult to identify a successor to CMOS technology. Among these technologies, PCRAM requires large energy for its resistive switching behavior, FeRAM suffers from signal degradation in scaling process, and MRAM has high endurance but it scales poorly and consumes large power because of large write currents. We focus on RRAM technology because of its simple structure, fast switching operation, and device scalability [4].

RRAM uses passive two-port memristors as storage elements. We present the design and optimization of low-power high-performance multibit one-transistor one-memristor (1T1R) RRAM arrays. The contributions of this paper are as follows.

1) We present the performance and energy models for n-bit 1T1R RRAM cell designed using titanium dioxide (TiO$_2$)- and hafnium oxide (HfO$_2$)-based memristors. These models consider the two-step read/write operation and the nonlinear behavior of TiO$_2$- and HfO$_2$-based memristors. These performance and energy models have been validated against HSPICE simulations (HSS). As a part of the modeling effort, we have also developed a SPICE model for HfO$_2$-based memristors.

2) We present a detailed discussion of the design and optimization of multibit 1T1R RRAM cells with TiO$_2$- and HfO$_2$-based memristors, and we calculate the optimum number of bits/cell considering energy and performance constraints of the entire multibit RRAM array.

3) We propose a mechanism for read reliability optimization in multibit RRAMs where the read noise margin is maximized using nonuniform memristor state assignment. We also compare the read energy consumption of multibit RRAM cells considering both nonuniform and conventional uniform memristor state assignments.

4) Using the performance and energy models, we present a detailed analysis of the impact of process (P), voltage (V), and temperature (T) variations on the access time, energy consumption, and reliability of multibit RRAM cells. We determine the optimum number of bits per 1T1R RRAM cell for both TiO$_2$- and HfO$_2$-based memristors that provides reliable operation under process, voltage, and temperature (PVT) variations.

In the rest of this paper, an overview of the memristor technology is presented in Section II. Section III discusses the related efforts in designing memristor-based circuits and systems. The detailed discussion of individual 1T1R n-bit memory cell and the overall architecture of a memory array are presented in Section IV. This is followed by the description of the performance models and energy models for read/write operation of the RRAM array, and the RRAM array’s design...
TABLE I
COMPARISON BETWEENFLASH MEMORY AND CURRENT EMERGING NONVOLATILE MEMORY TECHNOLOGIES

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<tr>
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<tbody>
<tr>
<td>R/W time (nsec)</td>
<td>IT</td>
<td>IT/IR</td>
<td>IT/IR</td>
<td>IT/IC</td>
<td>IT/IR</td>
</tr>
<tr>
<td>R/W energy (J/it)</td>
<td>60e3/2e6</td>
<td>376/20e3</td>
<td>1.3</td>
<td>200/134</td>
<td>8.5/10</td>
</tr>
<tr>
<td>Endurance</td>
<td>10^7</td>
<td>10^7</td>
<td>10^16</td>
<td>10^13</td>
<td>10^8</td>
</tr>
<tr>
<td>Retention</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
</tr>
<tr>
<td>Density (M/cm^2)</td>
<td>555</td>
<td>15.7</td>
<td>3.5</td>
<td>0.93</td>
<td>6.66</td>
</tr>
<tr>
<td>Tech. node (nm)</td>
<td>34</td>
<td>58</td>
<td>90</td>
<td>130</td>
<td>180</td>
</tr>
</tbody>
</table>

Fig. 1. Physical structure of (a) TiO_2-based memristor between two point contacts consisting of a highly conductive doped region and a highly resistive undoped region, where L is the thickness of the memristor and W is the thickness of the conductive region. (b) HfO_x-based memristor showing conductive filament (CF) growth/narrowing process where φ_min and φ_max are the minimum and maximum filament diameters, respectively.

and optimization in Section V. In Section VI, we explain the impact of PVT variations on the functionality of the multibit RRAM cells followed by concluding remarks in Section VII.

II. MEMRISTOR DEVICE TECHNOLOGY

Memristors provide a functional relationship between the charge and flux, which was first postulated in [10]. Several different implementations of memristors have been proposed in the literature. In this paper, we focus on TiO_2- and HfO_x-based memristor implementations. A detailed discussion of the alternate implementations of the memristors is presented in Section III.

The TiO_2-based memristor was first fabricated by Hewlett Packard [11]. The fabricated prototype had a highly resistive thin layer of TiO_2 and a second conductive deoxygenized TiO_2-x layer [Fig. 1(a)]. The change in the oxygen vacancies because of a voltage applied across the memristor modulated the dimension of the conductive region in the memristor. This resulted in a HRS and a LRS corresponding to the resistive and conductive regions of operation, respectively. We have summarized the equations required to model the TiO_2-based memristor functionality in Table II. The effective memristance of the memristor device can be calculated using (1) (proposed in [11]). Here, x(t) is the state of the memristor [12] [calculated using (3)], ω(t) is the thickness of the conductive doped region as a function of time, and L is the memristor thickness.

The rate of change of the memristor state follows the ionic drift model, which is a function of the memristor physical parameters and the current through the memristor. As the current itself varies with time, the change of memristor state exhibits nonlinear behavior. This nonlinear behavior can be expressed using a window function shown in (5) [12]. In (5), μ_0 ≈ 3 × 10^{-9} m^2/s/V [13] is the average dopant mobility and F(x(t), p) is the window function, where the parameter p controls the memristor nonlinearity. Increasing p yields a flat window function for larger memristor states. Window functions that consider the linear ionic drift, and the nonlinear behavior that appears at the boundaries of the memristor state, have been proposed in [14] and [15]. Both these window functions, however, get stuck at the memristor state boundaries. We use the window function proposed in [16] for developing the performance and energy models of the TiO_2-based RRAM cell. This function models the nonlinear behavior of the rate of change of state without getting stuck at the boundaries and is given in (7). Here, sgn is a sign function that prevents the state of the cell from getting stuck at the borders.

In case of the HfO_x-based memristor, the set/reset (changing memristor resistance to R(set)/R(reset)) process is performed by increasing/decreasing the diameter of the CF using positively charged oxygen vacancies (V_O) or Hf ions migration in a thermally activated hopping process in the filament growth model [17]. Applying a voltage across the HfO_x-based memristor forces the positive ions to move along the direction of the electric field while increasing the maximum temperature along the CF and changing the effective cross-sectional diameter of the CF [Fig. 1(b)]. This rate of change of diameter was derived in [17] and is given by

$$\frac{dφ}{dt} = Ae^{-\frac{E_{A0} - eV}{kT}}$$

where φ is the CF diameter, A is a pre-exponential constant, E_{A0} is the energy barrier for ion hopping, α is the barrier lowering coefficient, q is the elementary charge, V is the applied voltage across the memristor, k is the Boltzmann constant, T is the room temperature, ρ is the electrical resistivity, and k_{th} is the thermal conductivity. A similar expression with a negative rate of change is used for modeling the reset process in HfO_x-based memristors. As voltage is applied across the HfO_x-based memristor, its cross-sectional area changes and the instantaneous resistance of the CF changes according to $R(t) = 4ρL/πφ(t)^2$. The rate of change of the diameter for HfO_x-based memristors in filament growth model for set and reset operations is shown in Fig. 2. The nominal parameter values of the memristor used for generating this plot are
TABLE II
EQUATIONS USED TO MODEL TiO$\textsubscript{2}$- AND HfO$\textsubscript{x}$-BASED MEMRISTORS. $x(t)$ IS THE NORMALIZED STATE OF THE MEMRISTOR, $dx/dt$ IS THE RATE OF CHANGE OF STATE, AND $i(t)$ IS THE CURRENT THROUGH THE MEMRISTOR. $F(x(t), p)$ IS THE WINDOW FUNCTION, WHERE $p$ IS THE CONTROL PARAMETER. $R_{\text{ON}}$ AND $R_{\text{OFF}}$ ARE THE MINIMUM AND MAXIMUM MEMRISTANCES (ALSO KNOWN AS LOW RESISTANCE STATE (LRS) AND HIGH RESISTANCE STATE (HRS)), RESPECTIVELY, AND $\beta = R_{\text{OFF}}/R_{\text{ON}}$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$\text{TiO}_2$-based memristor</th>
<th></th>
<th>$HfO_x$-based memristor</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Memristance</td>
<td>$M(t) = R_{\text{ON}}x(t) + R_{\text{OFF}}(1 - x(t))$</td>
<td>(1)</td>
<td>$M(t) = R_{\text{ON}}x(t) + R_{\text{OFF}}(1 - x(t))$</td>
<td>(2)</td>
</tr>
<tr>
<td>Memristor state</td>
<td>$x(t) = \phi(t)/L$</td>
<td>(3)</td>
<td>$x(t) = C \left(1 - \frac{\phi_{\text{min}}^2}{\phi(t)^2}\right)$, $C = \frac{\phi_{\text{max}}^2}{\phi_{\text{max}}^2 - \phi_{\text{min}}^2} = 1 - 1/\beta$</td>
<td>(4)</td>
</tr>
<tr>
<td>Rate of change of state</td>
<td>$\frac{dx}{dt} = \frac{\mu R_{\text{ON}} i(t) F(x(t), p)}{L}$</td>
<td>(5)</td>
<td>$\frac{dx}{dt} = 2\phi(t) F(x(t)) \frac{dx}{dt}$</td>
<td>(6)</td>
</tr>
<tr>
<td>Window function</td>
<td>$F(x(t), p) = 1 - (x \pm \text{sgn}(-i(t)))^{2p}$</td>
<td>(7)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

![Fig. 2. Rate of diameter change for HfO$\textsubscript{x}$-based memristors in a filament growth model [17] for set ($V > 0$) and reset ($V < 0$) operations as a function of voltage across the memristor.](image)

### TABLE III

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$\text{TiO}_2$</th>
<th>$HfO_x$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{ON}}$ ($\Omega$)</td>
<td>100</td>
<td>3K</td>
</tr>
<tr>
<td>$R_{\text{OFF}}$ ($\Omega$)</td>
<td>16K</td>
<td>10M</td>
</tr>
<tr>
<td>$L$ (nm)</td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>$E_{\text{A0}}$ (eV)</td>
<td>-</td>
<td>1.2</td>
</tr>
<tr>
<td>$A$ ($m^{-1}$)</td>
<td>-</td>
<td>1</td>
</tr>
<tr>
<td>$\rho$ ($\mu\Omega\text{cm}$)</td>
<td>-</td>
<td>0.3</td>
</tr>
<tr>
<td>$k_{sh}$ ($Wm^{-1}K^{-1}$)</td>
<td>-</td>
<td>400</td>
</tr>
</tbody>
</table>

The rate of change of the HfO$\textsubscript{x}$-based memristor state is modeled as a voltage-controlled current source, and the combination of sgn functions guarantees the reliable set/reset operations, and the normalized memristor state does not get stuck when approaching one or zero.

III. RELATED WORK

Several oxide-based memristor devices have been proposed as storage elements in the design of RRAM arrays. HfO$\textsubscript{x}$ and TaO$\textsubscript{x}$ have been widely used as switching elements in RRAM cells [19]. Although several fabricated RRAM prototypes based on different switching materials have been reported in the literature, only a few reliable device models have been proposed for large-scale circuit-level simulations [17], [20]. A numerical model of filament growth based on thermally activated ion migration, which accounts for the resistance switching characteristics is proposed in [17]. This model (primarily developed for HfO$\textsubscript{x}$-based 1T1R cell) matches the measurement results for different metal–oxide RRAM configurations (HfO$\textsubscript{x}$/ZrO$\textsubscript{x}$ and NiO). The variation of switching parameters in RRAM devices using a trap-assisted
tunneling current solver considering the stochastic generation and recombination of oxygen vacancies is proposed in [21]. The compact model for the proposed RRAM switching behavior in [21] is introduced in [22], while the measurement results of the HfO$_2$-based prototypes verify this model in [23].

There are multiple efforts in place to develop accurate analytical model (AM) and SPICE model for the two-terminal memristor elements [17], [24], [25]. An analytical TiO$_2$ memristor model and the corresponding SPICE code that express both the static transport tunneling gap width and the dynamic behavior of the memristor state based on the measurement results are proposed in [24] and [26], respectively. In [27], a simplified yet accurate AM for the TiO$_2$ tunnel barrier phenomena analyzed in [24] with improved run times was developed. In [16], the authors developed a mathematical model for the prototype of memristor reported in [11] with dependent voltage and current sources as well as an auxiliary capacitor, which functions as an integrator to calculate the state of the memristor. In [28], a schematic diagram of the memristor SPICE macromodel based on a simplified window function for the rate of change of state was presented. A magnetic flux controlled SPICE model for memristors is proposed in [29] based on an exponential relationship for memristor $I$–$V$ characteristics.

Several memory circuit/architecture topologies have been proposed in the literature based on the memristive structures. In [30], a Si-based memristive system to fabricate high-density crossbar arrays with high yield and OFF/ON ratio is used. A memristor-based TiO$_2$ memory cell is introduced in [31] and its functionality is evaluated using system-level simulations. An energy-efficient dual-element TiO$_2$-based memory structure is proposed in [32], in which each memory cell contains two memristors that store the complementary states. Similarly, a 2-b storage memristive cell is proposed in [33]. Both these multibit memory cells have large area. Content addressable memory designed using TiO$_2$ memristors has been introduced in [12]. A memristor-based lookup table design has been introduced in [34] to replace the static RAM (SRAM)-based field-programmable gate array (FPGA) design while achieving higher density. In [35], the functionality, performance, and power of several CMOS/memristor-based circuits with memristor applications have been verified using a simulator based on a modified nodal analysis. An analysis of the peripheral circuitry of the crossbar array architecture is presented in [36]. A nonvolatile 8T2R SRAM cell that uses two HfO$_2$-based 1T1R cells along with the conventional 6T SRAM structure is introduced in [4] for low-power mobile applications. A bridge-like neural synaptic circuit with five TiO$_2$-based memristors, which is capable of performing sign/weight setting and synaptic multiplication operations, is introduced in [37]. In [38], the authors proposed adaptive write and read circuits for RRAM arrays to enhance yield and $\beta$ ratio while eliminating large power consumption rising from the resistance fluctuations.

Memristors are highly vulnerable to process variation and several authors have analyzed its impact on the functionality of the memristive structures. Line-edge roughness (LERs) caused by uncertainties in the process of lithography and etching [39], oxide thickness fluctuations (OTFs) caused during sputtering or atomic layer deposition, and random discrete doping (RDDs), which leads to randomness in resistivity of the conductive as well as the resistive region of the memristor, are generally the main causes of process variations. In [40], the effect of cross-sectional area and oxide thickness variations on the memristor resistance was analyzed. In [41], the effect of LER and OTF on the state $x(t)$, the rate of change of state $dx(t)/dt$, and power dissipation variations of TiO$_2$-based memristor was analyzed. Using an error correcting code design for conventional dynamic RAM (DRAM) memory, the authors in [42] propose the detection and mitigation of errors rising from process variations in both MOS-based and crossbar memristive RRAM cells. In [43], a parallel–series reference cell scheme to decrease the reference current fluctuations in 1T1R RRAM structure was used. Moreover, using a process-temperature-aware dynamic bitline (BL) bias circuit, they lower the read disturbance caused by BL voltage variations.

IV. $n$-Bit 1T1R RRAM Cell Design and Array Architecture

In this section, we provide a detailed discussion for the functionality of an $n$-bit 1T1R RRAM cell followed by a description for the architecture of a memory array designed using this RRAM cell as the building block. We discuss the implementation of memory cells and arrays using both TiO$_2$- and HfO$_2$-based memristors.

A. RRAM Cell Design

The circuit of the 1T1R RRAM cell is similar to a DRAM cell and consists of an access transistor and a memristor as storage element. Similar to DRAM, the access transistor is enabled for both read and write operations. As the memristor device shows considerable nonlinearity when approaching the states of zero ($R_{\text{on}} = R_{\text{off}}$) and one ($R_{\text{on}} = R_{\text{off}}$), it increases the required set/reset operation times at the two boundaries. We therefore ignore the states smaller than 0.1 and larger than 0.9 for faster set/reset, i.e., write operations. The 3 bits of a cell are stored in the 2$^n$ distinct subranges in the range 0.1–0.9. For an $n$-bit cell design, the state assignment can be done such that maximum noise margin would be achieved. For example, for a 2-b RRAM cell, a memristor state below 0.3 corresponds to 00, a memristor state between 0.3 and 0.5 corresponds to 01, a memristor state between 0.5 and 0.7 corresponds to 10, and a memristor state above 0.7 corresponds to 11. We refer to this assignment as a uniform state assignment. A nonuniform state assignment could also be used for the $n$-bit cell. A comparison of the two assignments is presented in Section VI.

To perform the read operation, the loadline (LL) is driven to charge the BL through the memristor and access transistor. The read operation of the $n$-bit RRAM cell may be destructive and could require periodic refreshing of the cell data. For threshold-based memristor technologies, recent measurement results have shown that if the drive voltage is less than a threshold, the state does not change for fast read operations (Fig. 2). The TiO$_2$ RRAM—based on the ionic drift model—is not a threshold-based technology [27] and shows more
d destructive during read cycles. A detailed analysis of the read destructive in multibit RRAM cells is proposed in Section V-A.

The write operation always consists of two suboperations—read followed by write as we need to know the data currently stored in the cell to determine the exact voltage that needs to be applied across the memristor to write new data. To perform the write operation, a positive or negative voltage is applied across the memristor for transitions to higher or lower states, respectively. The current flowing through the memristor changes the size of conductive region (in ionic drift model) or the diameter of the conductive filament (in filament growth model), thus increasing or decreasing the memristance. In the rest of this paper, we refer to the memory read and write operations as readtop and writetop, and the suboperations as readsub, refreshsub, and writesub. Thus, readtop = readsub + refreshsub, whereas writetop = readsub + writesub.

B. RRAM Array Architecture

The overall architecture of a memory array built using 1T1R RRAM cells is similar to the conventional DRAM array, i.e., a wordline (WL) is used to select a row of cells, and a BL is shared by the cells in a column for reading/writing (Fig. 3). In a RRAM array architecture, to perform the readsub operation, we first discharge the BL to 0 V, and then enable the WL and LL are enabled, the BL charges to one of the 2\(n\) possible transitions for the \(n\)-bit RRAM cell) needs to be applied across the memristor. For example, a 2-b/cell array needs 12 V corresponding to 12 different transitions. The refreshsub operation would be similar to the writesub operation and the applied voltage will depend on the mechanism used for refresh operation. A 2n-bit multiplexer-based digital-to-analog converter (DAC) can be used to generate the voltages to be applied across the memristor for refresh/refreshsub operation. During writesub/refreshsub operation, the outputs \(B_{0}^{\text{out}}\) and \(B_{n-1}^{\text{out}}\) are connected to the \(B_{0}^{\text{in}}\) and \(B_{n-1}^{\text{in}}\) inputs (corresponding to the current stored bits) and the data to be written into the cell are connected to the \(B_{0}^{\text{in}}\) and \(B_{n-1}^{\text{in}}\) inputs of the 2n-bit DAC. This ensures the DAC generates the correct voltage to be applied to the BL for writing the data. For the 2-b/cell array, we need a 4-b DAC that generates 12 different set/reset voltages and an ADC with three sense amplifiers.

V. PERFORMANCE AND ENERGY MODELS FOR 1T1R RRAM ARRAY

In this section, we discuss our performance and energy models for the \(n\)-bit 1T1R memory arrays designed using TiO2- and HfOx-based memristors. The parameters of TiO2- and HfOx-based memristors that are used in modeling and HSs are summarized in Table III.

A. Performance Models

As discussed in Section IV-A, the readtop and writetop operations of the \(n\)-bit 1T1R cell consist of readsub + refreshsub and readsub + writesub operations, respectively. The equivalent circuit model for the 1T1R RRAM cell during readsub operation is shown in Fig. 4. Here, \(R_{\text{m}}\) is the equivalent time-variant resistance of the memristor and \(R_{\text{ch}}\) is the access transistor channel resistance while operating in the triode region. The transmission gate, which is part of the predischarging path of the BL capacitor, is not included here as that transmission gate is switched OFF as soon as BL is discharged resulting in very high equivalent resistance for the transmission gate. \(C_{\text{BL}}\) and \(C_{d}\) are the BL capacitor and access transistor junction capacitor, respectively. In addition, \(R_{\text{BL}}\) is the total resistance of the BL. The BL voltage at the end of readsub operation (i.e., after time \(T_{R}\)) will be

\[
V_{\text{BL}} = V_{\text{LL}} \left(1 - e^{-\frac{T_{R}}{R_{\text{BL}}+R_{\text{ch}}+0.5R_{\text{BL}}C_{\text{BL}}}}\right).
\]

Here, the time constant of the junction capacitor \((C_{d})\) is much smaller than that of the BL capacitor \((C_{\text{BL}})\), and hence \(C_{\text{BL}} + C_{d}\) has been approximated to be equal to \(C_{\text{BL}}\). In addition, the term 0.5 \(R_{\text{BL}}C_{\text{BL}}\) is the intrinsic time constant of the BL modeled as a distributed RC-line. We assume the BL, WL, and LL to be 1-mm long, each with total capacitance of 200 fF and total resistance of 6.5 kΩ corresponding to copper metal line with 50 nm × 50 nm cross-sectional area.

![Fig. 3. n-bit/cell RRAM array architecture.](image-url)
In addition, we assume the distributed \( RC \)-line model with 80 segments for all of the interconnects in the RRAM array architecture. As an example, for a 2-b RRAM cell, (9) can be used to define the three reference voltages \( V_{\text{ref}1}, V_{\text{ref}2}, \) and \( V_{\text{ref}3} \) to be the input to the three sense amplifiers that are used to differentiate between the four different stored values while performing read\(_{\text{sub}}\) operation. The BL voltage depends on the data stored in the memristor, i.e., the memristor state. For \( V_{\text{ref}1} > V_{\text{BL}} \), \( V_{\text{ref}1} < V_{\text{BL}} \), \( V_{\text{ref}2} < V_{\text{BL}} < V_{\text{ref}2} \), and \( V_{\text{ref}2} < V_{\text{BL}} < V_{\text{ref}3} \), and \( V_{\text{ref}3} < V_{\text{BL}} \), the stored data is 00, 01, 11, and 10, respectively. We use Gray coding to increase the robustness and minimize the probability of getting 2-b error in the read operation. In Table IV, we compare the reference voltages calculated using the AM shown in (9) and using HS using 22-nm Predictive Technology Model [45]. Here, the read time of 1, 2 ns (for TiO\(_2\)) and 200, 400 ns (for HfO\(_x\)) is chosen based on the nominal \( \beta \) value for the two types of memristors in Table III. HfO\(_x\) has larger \( \beta \) and \( R_{\text{OFF}} \) values compared with TiO\(_2\), and therefore, it needs higher read time for reliable read operation.

To ensure a reliable read operation, there should be sufficient difference in the four different voltages developed on the BL corresponding to the four different data that can be stored in the 2-b cell. For very large BL voltage development times, the BL can get completely charged to the LL voltage \( V_{\text{LL}} \). Simultaneously, for very small BL voltage development times, the difference in the BL voltages may not be large enough for the sense amplifier to correctly determine the data stored in the cell. The BL voltage of TiO\(_2\)- and HfO\(_x\)-based 2-b/cell RRAM cells for various BL voltage development times during read operation are shown in Figs. 5 and 6, respectively. For our 2-b/cell RRAM array example, we design our sense amplifier such that it needs at least 12.5-mV differential inputs. Hence, we need at least 25-mV difference between the adjacent BL voltages corresponding to the four different data that can be stored in the 2-b cell. The \( V_{\text{ref}} \) inputs to the three sense amplifiers are chosen based on BL voltages (corresponding to the four different data that can be stored in the cell) while ensuring the 12.5-mV differential input. From Figs. 5 and 6, we choose the minimum read access time that ensures 12.5-mV differential voltage at the sense amplifiers. Therefore, for the TiO\(_2\)-and HfO\(_x\)-based 2-b/cell RRAM cells, we choose 1 and 200 ns. In the TiO\(_2\)-based cell, for the 1-ns read access time, the four different BL voltages are 125, 150, 186, and 245 mV. The corresponding \( V_{\text{ref}1}, V_{\text{ref}2}, \) and \( V_{\text{ref}3} \) values are 137.5, 168, and 215.5 mV, respectively. Similarly, in the HfO\(_x\)-based cell, for the 200-ns read access time, the four different BL voltages are 82, 107, 154, and 274 mV. The corresponding \( V_{\text{ref}1}, V_{\text{ref}2}, \) and \( V_{\text{ref}3} \) values are 94.5, 130.5, and 214 mV, respectively. The read times as a function of number of bits/cell \( n \) is shown in Fig. 7. These read times have been chosen using the same approach as described above for the 2-b/cell RRAM cell. As the value of \( n \) increases, we need larger read times to ensure the reliable read operation.

As discussed in Section IV-A, the read\(_{\text{sub}}\) operation of the 1T1R cell can be destructive. The read destructiveness of TiO\(_2\)-based memristors is larger compared with HfO\(_x\)-based memristors for the same LL voltage \( V_{\text{LL}} \). The TiO\(_2\)-based memristor therefore needs to be refreshed more frequently than HfO\(_x\)-based memristor. Considering the rate of change of state for TiO\(_2\) RRAM in (5), the number of consecutive read operations that will not destruct the stored data in multibit TiO\(_2\)-based 1T1R RRAM cell, i.e., the refresh threshold can be written as follows:

\[
\tau_{\text{ref-TiO}_2} \approx \frac{(x_{\text{max}} - x_{\text{min}}) (R_{m(x)} + R_{\text{ch}})}{2 \eta \gamma T_R V_{\text{LL}} (1 - (x - 1)^{2\eta})}.
\]  

Here, \( R_{m(x)} \) is the resistance of the memristor for each state, \( n \) is the number of bits/cell, \( T_R \) is the read access time, and \( x_{\text{max}} \) and \( x_{\text{min}} \) are the maximum and minimum normalized memristor states (0.9 and 0.1 in this paper), respectively, and \( \gamma = \mu_b R_{\text{ON}}/L^2 \). Large \( V_{\text{LL}} \), \( n \), and \( R_{\text{ON}} \) values (smaller \( \beta \)) necessitate more frequent refresh operation in the multibit RRAM cell. The contour plots of the number of consecutive nondestructive read operations in multibit TiO\(_2\) RRAM is shown in Fig. 8 for different \( n \) (number of bits/cell) and \( V_{\text{LL}} \) values for a memristor with initial state of \( x = 0.9 \). In case of the highly destructive multibit TiO\(_2\) memristor, we explored two different refresh schemes: a refresh operation

---

**TABLE IV**

Comparison between the Reference Voltages Determined Using AM and HS for a Read\(_{\text{sub}}\) Access Time of \( T_R(\text{TiO}_2) = 1, 2 \) ns and \( T_R(\text{HfO}_x) = 200, 400 \) ns in the 2-b/Cell 1T1R RRAM. \( V_{\text{LL}}(\text{TiO}_2) = 0.48 \) V and \( V_{\text{LL}}(\text{HfO}_x) = 0.7 \) V are chosen to reach to at least 25-mV Difference Between the Two Adjacent Reference Voltages. The Average Error Is 5.7% for TiO\(_2\) and 0.151% for HfO\(_x\).

<table>
<thead>
<tr>
<th>Reference Voltages</th>
<th>AM TiO(_2)</th>
<th>1 ns</th>
<th>HS TiO(_2)</th>
<th>1 ns</th>
<th>AM HfO(_x)</th>
<th>200 ns</th>
<th>HS HfO(_x)</th>
<th>200 ns</th>
<th>AM HfO(_x)</th>
<th>400 ns</th>
<th>HS HfO(_x)</th>
<th>400 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{\text{ref}1} )</td>
<td>137.5 mV</td>
<td>120.5 mV</td>
<td>162. mV</td>
<td>158.17 mV</td>
<td>94.5 mV</td>
<td>94.79 mV</td>
<td>100.85 mV</td>
<td>100.84 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{ref}2} )</td>
<td>168 mV</td>
<td>153.5 mV</td>
<td>190.4 mV</td>
<td>188.69 mV</td>
<td>130.5 mV</td>
<td>139.09 mV</td>
<td>135.25 mV</td>
<td>135.23 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{\text{ref}3} )</td>
<td>215.5 mV</td>
<td>202.5 mV</td>
<td>228.9 mV</td>
<td>231.37 mV</td>
<td>214. mV</td>
<td>214.6 mV</td>
<td>204.8 mV</td>
<td>204.81 mV</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
The corresponding contour plots of the number of consecutive nondestructive read operations for different \( n \) and \( V_{\text{LL}} \) values for a memristor with initial state of \( x = 0.9 \) are shown in Fig. 8. The threshold-based CF growth mechanism in HfO\(_x\) memristor makes it more resilient to read destructiveness compared with ion drift mechanism-based TiO\(_2\) memristors. As shown in Fig. 8, for small read voltage values, a large number of consecutive read operations are required to destruct the current state in multibit HfO\(_x\) RRAM technology. The refresh threshold proposed in (11) and shown in Fig. 8 exceeds the maximum allowed number of accesses (endurance) in the HfO\(_x\)-based RRAMs reported in [9] (Table I) and [4], which practically makes HfO\(_x\) as a nondestructive memristor technology at small read voltages. In case, large voltages are used for read\(_{\text{sub}}\) operation, then we might observe destructiveness of memristor state. To combat this, we propose to use a counter that tracks the current state of the memristor as well as the number of consecutive read operations. A refresh operation is done once the number of read operations exceeds the threshold given by (11). If we ignore the destructiveness (changing the memristance) during read\(_{\text{sub}}\) in the AM for simplicity, the resulting average error is 5.7% for TiO\(_2\) and 0.151% for HfO\(_x\).

The equivalent circuit model for the refresh\(_{\text{sub}}\)/write\(_{\text{sub}}\) operation of a 1T1R RRAM cell is shown in Fig. 4. For the TiO\(_2\)-based memristor, the refresh\(_{\text{sub}}\)/write\(_{\text{sub}}\) operation model uses the window function proposed in [16]. The switching time of the BL capacitor and the junction capacitor are the orders of magnitude lower than the switching time of the memristor. Hence, we do not consider these two capacitors in our AMs. Given the threshold voltage \( (V_{\text{th}}) \) drop across the access transistor (i.e., \( R_{\text{ch}} \)), the expression for memristor current during refresh\(_{\text{sub}}\)/write\(_{\text{sub}}\) operation is as follows:

\[
I_W(t) = \frac{V_{\text{BL}} - V_{\text{th}} - V_{\text{LL}}}{R_m(t)}
\]

Using the window function in (7) and the rate of change of state in (12), the refresh\(_{\text{sub}}\)/write\(_{\text{sub}}\) time can be approximated as

\[
T_W = \frac{R_{\text{OFF}} Q_i}{(V_{\text{BL}} - V_{\text{LL}} - V_{\text{th}})\gamma}
\]

where \( \gamma = \mu_i R_{\text{ON}}/L^2 \). Here, \( Q_i = \int_{x_i}^{x_i+1} 1 - x/1 - x^4 \, dx \) is the nonlinear delay integral for transitions to higher memristor states, where \( x_i \) is the state of memristor and \( Q_i = \int_{x_i}^{x_i+1} 1 - x/1 - (x - 1)^{4} \, dx \) is the nonlinear delay integral for transitions to lower memristor states (note that here \( Q_i \) could be negative leading to a negative voltage across the memristor for transitions to lower states). Here, the resistance of the memristor is approximated as \( R_m(t) \approx R_{\text{OFF}}(1 - x(t)) \) for simplicity. The integrals are determined from the window function we considered previously to model the nonlinearity of the memristor at the boundaries in (7) with \( p = 2 \). For the \( n \)-bit RRAM cell, the limits of the nonlinear delay integral \( Q_i \) will change based on \( 2^n \) different states. As an example, for the 2-b cell, we compared the required BL voltages for 12 possible write\(_{\text{sub}}\) transitions for 100- and 200-ns period in TiO\(_2\)-based 1T1R memory cells in Fig. 9. The \( V_{\text{LL}} \) voltage is maintained at 1.5 V for all the transitions. The average error between the
The average error is 9.81% for TiO$_2$-based cell and 5.19% for HfO$_x$-based cell, whereas for energy dissipation, the average error is 8.71% for TiO$_2$-based cell and 5.25% for HfO$_x$-based cell.

AM and the HS results for a 2-b TiO$_2$-based 1T1R memory cell is 9.81%.

For the HfO$_x$-based memristor using the rate of change of different states and 0%–90% distributed RC-line transition time for BL ($R_{\text{BL}}C_{\text{BL}}$), which will later be included in the whole RRAM array design specification. Comparing results from the AM and the HS for 1- and 2-ns period for a 2-b HfO$_x$-based 1T1R memory cell in Fig. 9, the average error is 5.19%. The modeling error for HfO$_x$-based cell is different from the TiO$_2$-based cell because different electrical parameters were used for each type of cell, as summarized in Table III.

The contour plots for the set time constraints of 2-b/cell TiO$_2$-based and HfO$_x$-based RRAM are shown in Fig. 10. Write speed is limited by the voltage applied across the memristor ($V_{\text{mem}}$). The write operation of HfO$_x$-based memristor is faster compared with TiO$_2$-based because of the faster rate of change of state for HfO$_x$ memristors.

B. Energy Models

In this section, we present the models for energy consumption during read$_{\text{sub}}$ and write$_{\text{sub}}$/refresh$_{\text{sub}}$ operations. It should be noted that the energy consumed in the WL, BL, and LL depends on the aspect ratio of the memory array. Once the array structure is finalized, the energy can be determined based on BL capacitance ($C_{\text{BL}}$), LL capacitance ($C_{\text{LL}}$), and WL capacitance ($C_{\text{WL}}$). The energy dissipated in the cell during read$_{\text{sub}}$ operation (for both TiO$_2$ and HfO$_x$) can be expressed as

\[
E_R = \int_0^{T_R} V_{\text{LL}}i_R(t) \, dt
\]

where $i_R(t)$ is the memristor current during the read$_{\text{sub}}$ operation. Using the RC circuit model in Fig. 4, the energy dissipated in the $n$-bit RRAM cell at the end of read$_{\text{sub}}$ operation will be

\[
E_R = C_{\text{BL}}V_{\text{LL}}^2 \left(1 - e^{\frac{-T_R}{R_{\text{mem}}C_{\text{BL}}}} \right)
\]

Table V compares the energy dissipation calculated from the AM and determined using HS during read$_{\text{sub}}$ operation of a 2-b TiO$_2$-based RRAM cell having a latency of 1 ns as well as a 2-b HfO$_x$-based RRAM cell having a latency of 200 ns for different stored data values. The average error is 8.44% and 0.038% for TiO$_2$ and HfO$_x$, respectively.

The read energy contour plots for different number of bits/cell for both TiO$_2$- and HfO$_x$-based RRAMs are shown in Fig. 11. For each value of bits/cell and each read timing constraint, we find the $V_{\text{LL}}$ value that gives at least 25-mV difference between two adjacent reference voltages of the sense amplifiers for reliable read operation. The difference between the reference voltages of the sense amplifiers is determined by the offset voltage of the input transistors in the voltage sense amplifiers and could be further reduced by increasing area at the expense of power [46]. Higher number of bits/cell requires larger drive voltages to increase read noise Margin, and therefore consumes more energy during read operation.
energy integral

The refresh sub/write sub operation in the TiO$_2$-based cell is lower amount of energy. Larger read times require lower drive voltages and dissipate

Fig. 10. Contour plots for set time (nanoseconds) in the 2-b/cell TiO$_2$-based (left) and HfO$_2$-based (right) RRAMs.

### Table V

<table>
<thead>
<tr>
<th>Cell Data</th>
<th>AM TiO$_2$</th>
<th>HS TiO$_2$</th>
<th>AM HfO$_2$</th>
<th>HS HfO$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>12.03 fJ</td>
<td>12.84 fJ</td>
<td>11.51 fJ</td>
<td>11.50 fJ</td>
</tr>
<tr>
<td>01</td>
<td>14.40 fJ</td>
<td>15.58 fJ</td>
<td>15.03 fJ</td>
<td>15.02 fJ</td>
</tr>
<tr>
<td>11</td>
<td>17.91 fJ</td>
<td>19.68 fJ</td>
<td>21.65 fJ</td>
<td>21.65 fJ</td>
</tr>
<tr>
<td>10</td>
<td>23.57 fJ</td>
<td>26.48 fJ</td>
<td>38.47 fJ</td>
<td>38.47 fJ</td>
</tr>
</tbody>
</table>

Larger read times require lower drive voltages and dissipate lower amount of energy.

The instantaneous current of the memristor while performing refresh sub/write sub operation in the TiO$_2$-based cell is determined by (12). Considering the $V_{th}$ voltage drop across the access transistor, the energy dissipated in the cell during refresh sub/write sub operation can be calculated as

$$E_W = \int_0^{T_W} (V_{th} - V_{th} - V_{LL})i_W(t) dt$$

(17)

where $\int i_W(t) dt = P_t/\gamma$ and $P_t = \int_{x_i}^{x_{i+1}} dx/1 - x^4$ is the nonlinear energy integral for transitions to higher memristor states and $P_I = \int_{x_i}^{x_{i+1}} dx/1 - (x - 1)^2$ is the nonlinear energy integral for transitions to lower memristor states. The dissipated energy in the diffusion capacitor of the access transistor is ignored because it is much smaller than the overall cell energy. For the n-bit RRAM cell, the limits of the nonlinear energy integral $P_t$ will change based on $2^n$ different states.

Fig. 9 compares the energy dissipated in a 2-b 1TIR cell for write sub in 12 possible transitions calculated using the AM and the HS for TiO$_2$-based configurations with transition time of $T_W = 100$ and 200 ns. The average error is 8.71%.

The write sub/ref fresh sub energy in the HfO$_2$-based memristor is modeled as

$$E_W = \int_0^{T_W} V^2/R(t) dt$$

(18)

where $V$ is the voltage across the memristor. Here, using $R(t) = (1 - x(t)/C)R_{OFF}$, the closed form expression for write sub/ref fresh sub energy in n-bit 1TIR HfO$_2$-based cell is

$$E_W = \frac{V^2\phi_{min}(\frac{d\phi}{dt})^{-1}}{2C R_{OFF}} S_i$$

(19)

where $S_i = \int_{x_i}^{x_{i+1}} dx/(1 - x^2)^{1/2}$ is the nonlinear energy integral for HfO$_2$-based memristors. Because there is a threshold voltage drop across the access transistor, the write voltage ($V$) in (19) is chosen as one threshold voltage below the difference between $V_{th}$ and $V_{LL}$ voltages. In the n-bit RRAM cell, the limits of the nonlinear energy integral $S_i$ will change based on $2^n$ different states. The average error between the dissipated energy of a 2-b HfO$_2$ RRAM cell model and the simulation results is 5.25% (Fig. 9). We do not consider the effect of subthreshold leakage in our energy analysis because all the transistors are working in strong inversion region of operation.

Using the energy models, we compare the different energy components of the 1TIR RRAM array for different number of bits/cell. The transition times of different components (other than the cell) in the RRAM array have been assumed constant for different number of bits and are 1.3 ns, 1.3 ns, 1 ns and 1 ns for wordline, loadline, ADC and Mux-based DAC, respectively. The energy consumption in different components of the RRAM array during read operation for TiO$_2$-based RRAMs is shown in Fig. 12. Cell energy increases during read operation for higher number of bits. This is due to higher LL voltages required for providing sufficient read noise margin for higher number of bits/cell. Because the read process of multibit TiO$_2$ RRAM is destructive (Fig. 8), we consider the energy of read, followed by a refresh operation in Fig. 12.

The total WL energy is constant across all the cells. The number of sense amplifiers increases with number of bits/cell ($2^n - 1$ sense amplifiers for n-bit RRAM cell), and hence the energy/bit of the sense amplifiers increases. The same trend is observed for the decoder energy as the number of multiplexers increases with the number of bits/cell.

To increase the read reliability of multibit RRAM array, we assume there should be at least 25-mV difference between two adjacent reference voltages. One way to reach this voltage difference is to use uniform state assignment and increase the $V_{LL}$ voltage. In the uniform state assignment scheme, there is a fixed distance between two adjacent states. Another way of reaching the 25-mV difference between two adjacent reference voltages is by lowering $V_{LL}$ voltages, and choosing the appropriate memristor states such that the read reliability would be maximized. This approach is called nonuniform...
state assignment where the 0.1–0.9 range for the state of a memristor is not uniformly shared between the $2^n$ different data that can be stored in the cell. Comparing uniform and nonuniform state assignment strategies, the nonuniform state assignment consumes lower energy because of lower $V_{LL}$ values. The minimum total read energy/operation is consumed at $n = 2$ for uniform state assignment and $n = 3$ for nonuniform state assignment. Considering the same throughput constraint (# bits/cell $n = 3$) for both cases, nonuniform state assignment consumes 32.1% less energy than uniform state assignment.

Using the same approach, we show the energy consumption in different components of the RRAM array during read operation for HfO$_2$-based RRAMs using uniform and nonuniform state assignments in Fig. 12. The refresh energy of the multibit HfO$_x$ memristor is amortized among different components of the array. Compared with TiO$_2$ and considering the same throughput constraint ($n = 3$), the total read energy consumption of the HfO$_x$ RRAM array using nonuniform state assignment is 59.07% lower.

The energy consumed in various components of the RRAM array during the write operation for both TiO$_2$- and HfO$_x$-based RRAMs is shown in Fig. 13. Because the size of mux-based DAC increases with number of bits/RRAM cell, the energy consumption of the DAC increases accordingly. The total WL and LL energies are constant across all the cells. We determine the cell energy using the average energy value of all possible transitions for the $n$-bit cell. The TiO$_2$ cell energy dominates the energy dissipated in all the array components because of large set/reset time and lower resistance values for TiO$_2$ RRAM, while the HfO$_x$ cell energy is much smaller than the energy in the remaining array components. The minimum total write energy/operation is consumed at $n = 3$ for both the cases.

VI. PVT VARIATION ANALYSIS OF n-BIT RRAM CELL

As shown in Section III, OTF and LER cause variations in memristor geometry [40], [41], [47] and RDD causes randomness in resistivity, which directly impacts the performance and energy dissipation of RRAM cells. In this section, we apply the Monte Carlo methodology [41] to our models for both TiO$_2$- and HfO$_x$-based memristors to analyze the influence of OTF, LER, and RDD on the performance and energy of the $n$-bit 1T1R RRAM cell. For our analysis, we exclude the variations in the energy and performance of the CMOS devices because of PVT variations to isolate and quantify the true impact of PVT variations on the memristors device functionality and the cell as a whole.

The LER of the memristor has been modeled as a combination of the low and high frequency domain disturbances in [41] and [48], and is given by

$$L_{ER} = L_{LF} \cdot \sin(f_{max} \cdot r) + L_{HF} \cdot z \quad (20)$$

where the sinusoid function with the amplitude of $L_{LF}$ describes the low-frequency domain variations. Here, $f_{max} = 1.8$ MHz is the mean of the low-frequency range with a uniform distribution represented as $r \in U(-1,1)$. $L_{HF}$ accounts for the high-frequency variations and $z$ is considered to have a normal distribution function as $N(0,1)$. The effect of OTF is usually modeled as a Gaussian distribution with a $\sigma = 2\%$ deviation from the nominal memristor thickness [40], [41]. In addition, RDD has been modeled as having a Gaussian distribution with $\sigma = 2\%$ [47] in the resistivity term in both ionic drift and filament growth models for TiO$_2$- and HfO$_x$-based RRAMs.

Considering the nominal parameters in Table III, we explore the effect of OTF, LER, and RDD on the states variations of both TiO$_2$- and HfO$_x$-based RRAMs. The state definition for ionic drift-based TiO$_2$ RRAM model is only a function for the ratio of the doped region to memristor thickness. The movement of dopants along the memristor thickness defines memristance [Fig. 1(a)]. Therefore, the state assignment will only be affected by OTF. In other words, LER and RDD will not change the state assignment of TiO$_2$-based RRAMs according to ionic drift memristor model. The impact of OTF on TiO$_2$-based RRAM with uniform and nonuniform state assignments for different number of stored bits ($1 \leq n \leq 4$) for 10,000 samples is shown in Fig. 14. The multibit TiO$_2$-based 1T1R RRAM cell is resilient to OTF-based process variations up to $n = 3$ for uniform state assignment and up to $n = 2$ for nonuniform state assignment, where no overlap is observed between the adjacent states.

The state definition for filament growth-based HfO$_x$ RRAM model is only a function of filament diameter. Therefore, the state assignment will only be affected by LER. OTF and RDD will not change the state assignment of HfO$_x$-based RRAMs. The uniform and nonuniform state distributions of the HfO$_x$-based RRAM for different number of stored bits ($1 \leq n \leq 4$) are shown in Fig. 15. The multibit HfO$_x$-based 1T1R RRAM cell is resilient to LER-based process variations.
Fig. 12. Energy dissipated in different components of the multibit TiO$_2$-based ($T_R = 1$ ns) (left plot) and HfO$_x$-based ($T_R = 200$ ns) (right plot) RRAM array in read operation for uniform (left bar) and nonuniform (right bar) state assignments.

Fig. 13. Energy dissipated in different components of TiO$_2$-based ($T_W = 100$ ns) (left) and HfO$_x$-based ($T_W = 1$ ns) (right) RRAM array in write operation.

Fig. 14. Variations in the uniform state assignment (left) and nonuniform state assignment (right) of the multibit TiO$_2$-based memristor caused by OTF. The memristor state distribution for each number of bits/cell is such that the maximum process noise margin would be achieved.

Fig. 15. Variations in the uniform state assignment (left) and nonuniform state assignment (right) of the multibit HfO$_x$-based memristor caused by LER. The memristor state distribution for each number of bits/cell is such that the maximum process noise margin would be achieved.

up to $n = 3$ where no overlap is observed between the adjacent states.

Table VI summarizes the effect of LER, OTF, and RDD on the state assignment, write time, write energy, read energy, and read destructiveness of the 3-b TiO$_2$- and HfO$_x$-based 1T1R cells. As discussed earlier, the TiO$_2$ memristor state is only affected by OTF, whereas the HfO$_x$ memristor state is only affected by LER. The impact of LER, OTF, and RDD is quantified as $(3\sigma/\mu) \times 100\%$ value of each parameter. OTF has higher impact on the TiO$_2$ specifications compared with LER.
In addition, OTF has the highest impact on the write time variations for the multibit TiO$_2$ memristor because the TiO$_2$ set/reset time is a quadratic function of memristor thickness based on (13). Similarly, the effect of OTF on the write energy and read destructiveness of the TiO$_2$ RRAM is higher than LER. The variation in read destructiveness changes the refresh threshold, which affects the reliability of read operation. OTF and LER have similar impact on read energy because it is mostly dominated by BL variations according to (16). It should be noted that OTF has a minimal impact on the write time and read destructiveness of the HfO$_x$-based 1T1R cell as these two parameters are independent of the oxide thickness [see (13) and (14)]. LER has the highest impact on the write energy variations of the multibit HfO$_x$ memristor because of its sensitivity to filament diameter fluctuations based on (19). The rate of change of diameter in the filament growth model has higher sensitivity to RDD at lower voltages. In other words, high set/reset voltages limit the effect of RDD in write time variations of HfO$_x$-based RRAMs. However, read destructiveness significantly changes with RDD because the applied read voltages are considerably low compared with write (set/reset) voltages, which deteriorates the read reliability of the HfO$_x$-based RRAMs.

The power supply noise in VLSI chips causes variations in the supply voltage applied to various transistors in a circuit, which in turn causes variations in performance and energy dissipation. Table VII summarizes the impact of voltage variations on write time, write energy, read energy, and destructiveness of a 3-b RRAM cell. Without loss of generality, we explore two cases where each voltage reference has been assumed to have a Gaussian distribution with $3\sigma = 6\%$ and $3\sigma = 10\%$ of the nominal value. We calculate the write time and energy variations considering 56 possible transitions for the 3-b 1T1R RRAM cell. The write time and write energy of the HfO$_x$ RRAM have more variations compared with TiO$_2$ because these two parameters are exponential functions of applied voltage in HfO$_x$ RRAM according to (14) and (19). Comparing the rate of state change in (5) and (6), the destructiveness of the HfO$_x$-based memristor state is considerably more sensitive to voltage fluctuations. This will significantly affect the refresh threshold in (11) (Table VII). The read energy has similar amount of variations because of voltage fluctuations for both the materials according to (16).

We also analyzed the impact of temperature variations on performance and energy metrics of both TiO$_2$- and HfO$_x$-based memristors in the 3-b RRAM cell. The temperature dependency of the ionic drift model has been modeled in [49] where thermal resistance of the filament, defined as the ratio between the maximum temperature increase in the filament and the dissipated electrical power [50], for the state 1 ($R_{\text{ON}}$) and state 0 ($R_{\text{OFF}}$) in the TiO$_2$ filament are derived as follows:

\[
R_{\text{th}}(R_{\text{ON}}) = L/(8k_M A_{\text{CF}}). \tag{21}
\]

\[
R_{\text{th}}(R_{\text{OFF}}) \approx (2\text{ArcSinh}[L/(\sqrt{A_{\text{CF}}})] - 1.5)/(4k_I L). \tag{22}
\]

Here, $k_M = 30$ W/mK and $k_I = 3$ W/mK [49] are the thermal conductances of the metal and insulator corresponding to titanium oxide thin films with oxygen vacancies conductive channels and $A_{\text{CF}}$ is the filament area. The change in resistance of the RRAM based on ionic drift model follows $\Delta R_{\text{RRAM}} \propto \Delta T/(R_{\text{th}} I^2)$, where $I$ is the RRAM current.

Table VIII summarizes the impact of temperature variations on write time, write energy, read energy, and destructiveness of both TiO$_2$- and HfO$_x$-based memristors in the 3-b RRAM cell. We explore two cases with nominal ambient temperature and variations of $\Delta T = 10$ K and $\Delta T = 30$ K. Temperature variations have a larger impact on the read destructiveness of the HfO$_x$-based memristor. The rate of change of diameter in HfO$_x$-based RRAMs because of temperature variations increases at lower applied voltages based on filament growth model in (8) [Fig. 16(a)]. The variations in write time and write energy of HfO$_x$ RRAM is higher than TiO$_2$ because of the exponential temperature term in these metrics for HfO$_x$ RRAM. The effect of temperature variation on the intermediate states of the multibit TiO$_2$ RRAM can be analyzed using the effective thermal resistance as $R_{\text{th}} = R_{\text{th}}(R_{\text{ON}})|R_{\text{th}}(R_{\text{OFF}})$ [49], where the corresponding cross-sectional area for each state is plugged into the two thermal resistance expressions in (21) and (22). The effective thermal resistance of a 3-b TiO$_2$-based RRAM is shown in Fig. 16(b).
for different memristor states. Temperature variations have minimal effect on the read energy fluctuations of TiO$_2$ RRAM because it is mostly affected by BL resistance (according to 9). This is, however, not the case for the HfO$_x$ RRAM because it is mostly affected by BL resistance (according to 9).

Fig. 16. (a) Diameter change of HfO$_x$-based memristors as a function of temperature for different applied voltages in filament growth model. Diameter shows higher variation with temperature at lower loadline voltages.

(b) Effective thermal resistance of a 3-bit TiO$_2$-based RRAM as a function of temperature for different applied voltages in filament growth model. Diameter shows higher variation with temperature at lower loadline voltages.

VII. CONCLUSION

In this paper, we presented the design and optimization of an n-bit 1T1R RRAM array designed using TiO$_2$- and HfO$_x$-based memristors. We first presented the models for the performance and energy of read and write operations in an n-bit 1T1R RRAM cells designed using TiO$_2$- and HfO$_x$-based memristors. A new SPICE netlist for HfO$_x$ memristors was proposed based on the change in the CF diameter. We validated our performance and energy models against HSSs, and the difference is less than 10% for both n-bit TiO$_2$- and HfO$_x$-based 1T1R cells. Using energy and performance constraints, we determined the optimum number of bits/cell in the multibit RRAM array to be three. The total write and read energy of the 3-bit TiO$_2$-based RRAM array was 4.06 and 188 fJ/b for 100 and 1 ns write and read access times, whereas the optimized 3-bit HfO$_x$-based RRAM array consumed 365 and 173 fJ/b for 1 and 200 ns write and read access times, respectively. We explored the tradeoff between the read energy consumption and the robustness against process variations for uniform and nonuniform memristor state assignments in the multibit RRAM array. Using the proposed models, we analyzed the effects of process, voltage, and temperature variations on performance and energy consumption and the reliability of n-bit 1T1R memory cells. Our analysis showed that multibit TiO$_2$ RRAM is more sensitive to OTF, whereas HfO$_x$ RRAM is more sensitive to LER and is more susceptible to voltage and temperature variations.

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