Performance and Energy Models for Memristor-based 1T1R RRAM Cell

Mahmoud Zangeneh and Ajay Joshi
Electrical and Computer Engineering Department, Boston University
Boston, MA, USA
{zangeneh, joshi}@bu.edu

Abstract

Sustaining the trend of lowering energy dissipation and read /write access time and increasing density in CMOS-based memory arrays is becoming extremely challenging with each new technology generation. Hence, alternate technologies that can supplant CMOS technology need to be explored. Memristor-based resistive memory with its scaling potential and endurance is one of the viable replacements to CMOS. This paper presents accurate analytical models for the performance and the energy dissipation of a 1-transistor 1- memristor (1T1R) resistive random access memory (RRAM) cell structure. We have verified our models against detailed HSPICE simulations and our models show that the time required to write logic one into the cell is typically 30% larger than the time required to write logic zero and is in the order of ns. Unlike the access time, the energy dissipation of the cell is the same for writing logic one and logic zero (less than 350 fJ/bit). The energy dissipated while reading is roughly 120 fJ/bit which is 65% less than the energy of writing.

Categories and Subject Descriptors
B.3.1 [MEMORY STRUCTURES]: Semiconductor Memories
Keywords
Memristor, Resistive memory, Modeling

1. INTRODUCTION

Access time, density and power dissipation of memory (on-chip static random access memory (SRAM), off-chip dynamic random access memory (DRAM) or Flash Memory) have a direct impact on the overall performance of a computing system. Over the years, complementary metal oxide semiconductor (CMOS) technology scaling made it possible to continuously decrease access time and energy consumption, and increase the density of memory blocks. However, maintaining this trend has become extremely challenging due to the limitations associated with scaling CMOS technology in the nanometer regime. To maintain reliable operation under the manufacturing variations in the nanometer regime, redundant circuits are required that increases power dissipation and decreases memory density. Moreover, any intermediate error detection or correction steps needed for reliable operation increases the memory access time.

It is therefore imperative to explore emerging devices for building memory arrays that have lower power dissipation, higher performance, higher density and reliable operation for future computing systems. Two-terminal memristor devices, with their excellent scaling potential ($< 10\ nm$) and endurance (> 10 billion cycles) [1], can be used as storage elements and are considered viable replacements to conventional CMOS-based memory designs. The memristor can be considered as a variable resistor which can be programmed by changing the voltage drop across the memristor or changing the current injected into the memristor. Here, programming amounts to changing the value of the 'memristance' which leads to two different states for the memristor. These two states can correspond to storage of logic 0 and logic 1 in the memristor.

In this paper we model and verify the performance and energy for reading and writing a non-volatile monolithically integrated hybrid CMOS/memristor memory cell consisting of 1 CMOS transistor and 1 memristor [2]. This 1-transistor 1-memristor (1T1R) resistive random access memory (RRAM) cell structure is similar to a DRAM cell – the data is stored as the resistance of the memristor, and the transistor serves as an access switch for reading and writing data. We chose the 1T1R cell as the basic building block for a non-volatile RRAM array as it avoids sneak path problems [3] and ensures reliable operation. The two main contributions of this paper can be summarized as follows:

- We have formulated the complete end-to-end functionality (read/write/refresh) of the 1T1R RRAM cell at the circuit level.
- We have developed analytical models for both performance and energy consumption during write operation and read operation of the 1T1R RRAM cell. These models have been validated against detailed circuit simulations using HSPICE.

The rest of the paper is organized as follows. Section 2 reviews the device-level aspects of the memristors, while Section 3 summarizes the memristor models and memristor-based memory cell designs proposed by other researchers. Section 4 explains the functionality of the non-volatile 1T1R RRAM cell. Sections 5 and 6 discuss the analytical models (development and validation) for the performance and energy consumption during read/write operation of the 1T1R RRAM cell, respectively. Section 7 concludes the paper.

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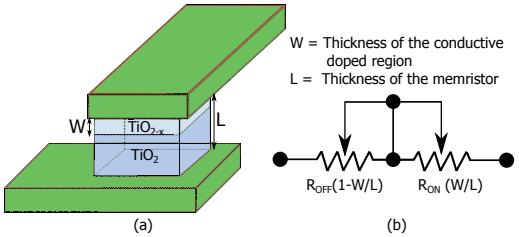

Figure 1: Variable resistor model for the memristor consisting of a highly conductive doped region and a highly resistive undoped region. (a) 3D view of the device. (b) Circuit-level model.

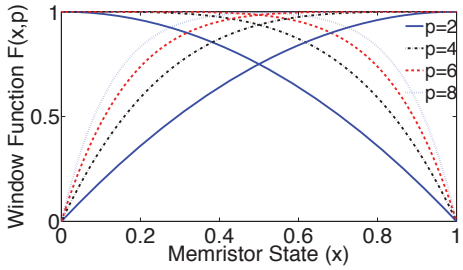

Figure 2: Dynamic window function of the memristor state showing the nonlinear behavior of the memristor for different control parameter p. The current sign function prevents the state from getting stuck at the two boundaries [6].

2. MEMRISTOR DEVICE TECHNOLOGY

Memristors provide a functional relationship between the charge and flux and was first postulated in [4]. The measurement results of a titanium dioxide nanoscale device that exhibited these memristive characteristics was first presented in [5]. The physical model for the memristor in [5] was specified by a time-dependent resistor whose value is linearly proportional to the charge q passing through it. The fabricated prototype introduced in [5] consists of a highly resistive thin layer of TiO_2 and a second conductive deoxygenized TiO_{2-x} layer (see Figure 1). The change in the oxygen vacancies due to a voltage applied across the memristor modulates the region of operation in the memristor. This results in two distinct states - a high resistance state and a low resistance state corresponding to the resistive and conductive region of operation, respectively. The effective 'memristance' of the memristor device can be calculated using Equation (1) proposed in [5].

$$M(t) = R_{ON}\frac{w(t)}{L} + R_{OFF}(1 - \frac{w(t)}{L}). \quad (1)$$

In Equation (1), R_{ON} and R_{OFF} are the minimum and maximum memristance, respectively, $w(t)$ is the thickness of the conductive doped region as a function of time, and L is the memristor thickness. The doped region is usually considered normalized to the memristor thickness [1] and is written as $x(t) = w(t)/L$, where $x(t)$ is called the state of the memristor. The rate of change of the memristor state is a function of the memristor physical parameters and the current through the memristor. As the current itself varies with time, the change of memristor state exhibits nonlinear behavior. This nonlinear behavior can be expressed using a window function as shown in Equation (2) [1].

$$\frac{dx(t)}{dt} = \frac{\mu_v R_{ON}}{L^2} i(t) F(x(t), p) \quad (2)$$

In Equation (2), $F(x(t), p)$ is the window function and the nonlinearity can be controlled with control parameter p. Increasing p yields a flat window function for larger memristor states. Also, μ_v is the mobility of the oxygen vacancy dopants. Various window functions have been proposed in the literature that consider the linear ionic drift and the nonlinear behavior which appears at the boundaries of the memristor state. A linear approximation of the dynamic behavior of the state is addressed in [7]. This model, however, gets stuck at the boundaries of the state. A modified function that considers the nonlinear behavior of the memristor is proposed in [8] where it still gets stuck once the state reaches the two boundaries. A new window function that models the nonlinear behavior of the rate in the state change without getting stuck at the boundaries is proposed in [6] and given in Equation (3). We use this window function for developing the performance and energy models of the 1T1R RRAM cell.

$$F(x(t), p) = 1 - (x - sgn(-i(t))^{2p}. \quad (3)$$

In Equation (3), $i(t)$ is the current through the memristor and sgn is a sign function that prevents the state of the cell from getting stuck at the borders. Figure 2 shows a plot of the window function for different p values.

3. RELATED WORK

There are multiple efforts in place to develop accurate models for the two-terminal memristor elements. An analytical TiO_{2-x} memristor model and the corresponding SPICE code that express both the static transport tunneling gap width and the dynamic behavior of the memristor state based on the measurement results are proposed in [9]. In [6], the authors developed a mathematical model for the prototype of memristor reported in [5] with dependent voltage and current sources as well as an auxiliary capacitor which functions as integrator to calculate the state of the memristor. The authors in [10] presented a schematic diagram of the memristor SPICE macromodel based on a simplified window function for the state change rate. However, most of these efforts use simplified analytical approaches and do not accurately consider the nonlinear behavior of the memristors. Moreover, not all of these models have been validated against measurement results. Several circuit topologies have been proposed in the literature based on the memristive structures. The authors in [11] used a Si-based memristive system to fabricate high-density crossbar arrays that can be addressed with high yield and ON/OFF ratio.

A read/write memristor based memory cell is introduced in [12] which utilizes purely system-level simulations to evaluate its functionality and lacks circuit-level verifications for the proposed closed-form expressions. An energy-efficient dual-element memristor-based memory structure is proposed in [13], in which each memory cell contains two memristors that store the complement states. Similarly, a 2-bit storage memristive cell is proposed in [14]. Both these multi-bit memory cells have large area overhead. Content addressable memory (CAM) design using memristors has been introduced in [1]. The simulation results and the measurements from the fabricated prototype of the proposed CAM cell are not yet verified. Hybrid logic circuits based on the crossbar/CMOS structures are physically viable and proposed in [15] and could offer function density of at least two orders of magnitude higher than that of their CMOS counterparts fabricated with the same design rules, at the same power density, but with higher logic delay [11]. An analysis on the peripheral circuitry of the crossbar array architecture is presented in [16]. We propose a 1T1R RRAM cell

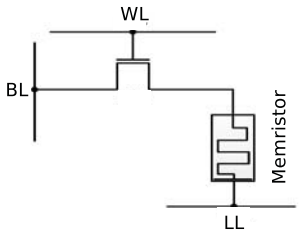

Figure 3: Schematic of the 1T1R RRAM cell. The capacitor of the conventional volatile DRAM is replaced with a memristor resulting in a nonvolatile memory cell.

based memory architecture. Unlike the proposed architecture in [16], the wordline or bitline drivers do not have direct access to the memristor. Hence, we do not have the issue of sneak paths that would be observed in the cross-point array architecture. We account for the access transistor and bitline parasitics to develop models for read/write access time and energy. We have validated our models against detailed HSPICE simulations.

4. 1T1R RESISTIVE RANDOM ACCESS MEMORY (RRAM) CELL

The difficulty associated with scaling SRAM, DRAM and Flash memory necessitates the exploration of emerging devices that can sustain the trend of lowering power, lowering access time and increasing density with each new generation. A non-volatile and low-power memory cell consisting of 1 CMOS transistor and 1 memristor is illustrated in Figure 3. This 1T1R RRAM cell stores data in the form of the resistance of the memristor element. The overall architecture of a memory array built using RRAM cells is similar to the conventional DRAM cell i.e. a wordline is used to select a row of cells, and a bitline is shared by the cells in a column for reading/writing.

During write operation, a voltage of V_{DD} is applied to the wordline, and a positive or negative voltage is applied across the memristor for writing logic 1 or logic 0, respectively. This voltage drop across the memristor is achieved by charging the bit line to V_{DD} (for logic 1) or discharging the bitline to 0 V (for logic 0) and applying a voltage of $V_{DD}/2$ at node LL. The write access time is dependent on the voltage drop across the memristor and the physical parameters of the memristor. While writing logic 1, the current flowing through the memristor increases the size of conductive region, thus reducing the 'memristance'. While writing logic 0, the current flowing through the memristor decreases the size of conductive region, thus increasing the 'memristance'. To read data out of the 1T1R cell we first discharge the bitline to 0 V, apply a voltage of V_{DD} to the wordline and apply V_{DD} to node LL. The pulse width on the wordline and loadline during reading is the same as read access time. For a fixed predefined time period, depending on the data stored in the cell (i.e. the resistance of the memristor), the bitline charges to a value that is above (for logic 1) or below (for logic 0) a threshold voltage. The bitline resistor and capacitor is calculated to be 6.8 $K\Omega$ and 200 fF for 1 mm bitline length, respectively. A differential sense-amplifier with V_{BL} as one input and threshold voltage as the other input is used to determine the value stored in the 1T1R RRAM cell. The sense amplifier has been designed to detect voltage differentials of 50 mV and larger. The read noise margin of the 1T1R RRAM cell is larger than other cell topologies,

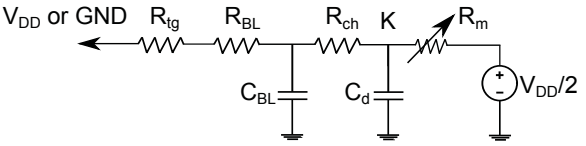

Figure 4: Equivalent circuit of the 1T1R cell in writing phase. V_{BL} is set to V_{DD} through a transmission gate switch while writing logic 1 and remains at zero while writing logic 0.

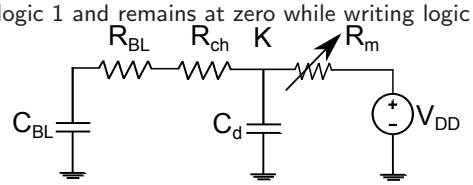

Figure 5: Equivalent circuit of the 1T1R cell in reading phase. The transmission gate switch is off while reading.

which lowers the required gain of the sense amplifier, leading to lower power consumption. Higher noise margins of the 1T1R cell particularly appear when smaller R_{ON} is chosen. This leads to larger R_{OFF}/R_{ON} ratios and larger reliabilities since the bitline voltage for reading logic 1 will increase and the following sense amplifier can distinguish between logic 1 and 0. Also increasing the memristor thickness will lead to higher noise margins since the rate of change of state will decrease according to Equation (2), leading to larger bitline voltages when reading logic 1. This will however increase the area of the 1T1R cell. An additional source of power saving during read operation is the discharging of the bitline to 0 V prior to reading as against the precharging operation performed for DRAM. It should be noted that during both read and write operation, we activate all the bitlines that share the selected wordline i.e. we read/write all the cells in the row. In case of architectures where only a part of the row is read/written, switches will need to be added onto the wordline and loadline. The unselected cells in the other rows are isolated using the CMOS access transistors.

5. PERFORMANCE MODELS

In this section, we present the models for read and write operation of a 1T1R RRAM cell. The proposed performance models can be used in the design exploration of a large memristive array architecture. The equivalent circuit model for the 1T1R RRAM cell during write operation is shown in Figure 4, while that for the read operation is shown in Figure 5. Here, R_m is the equivalent resistance of the memristor, R_{ch} is the access transistor channel resistance during writing/reading while operating in the triode region and R_{tg} is the transmission gate switch equivalent resistance which is used for pre-charging or pre-discharging the bitline capacitor. R_{BL}, C_{BL} and C_d are the bitline resistor, bitline capacitor and transistor junction capacitor, respectively.

5.1 Write Operation Model

The time required to change the state from 0 to 1 and 1 to 0 of a memristor that is directly connected to a voltage source was previously derived in [12] and is given by

$$T_w = \frac{L^2(1+\beta)}{2\mu_v V_A} \quad (4)$$

where β is the ratio of R_{OFF}/R_{ON} and V_A is the magnitude of the applied voltage. According to equation (4), the write time of a memristor, which is a function of physical parameters of the device, increases with increase in L and β and decreases with increase in applied voltage due to the increase

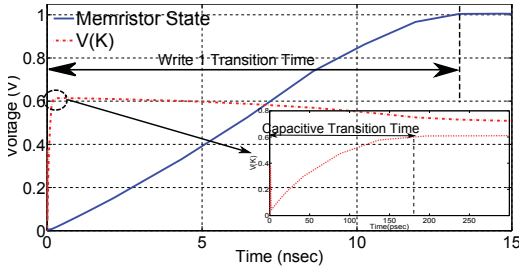

Figure 6: Variation of node "K" while writing logic 1. The write access time dominates the transient response of the bitline and parasitic cell capacitors.

in the injected flux into the device. This write model does not consider the nonlinearity of the change of state leading to an inaccurate estimation of the write time.

We use a 1T1R memory cell that avoids sneak path by isolating the memristor when not in use. The write operation model presented here for the 1T1R cell uses the window function proposed in [6]. Figure 6 shows the transient response of the node "K" (see Figure 4), where the charging time of bitline and transistor junction capacitors is less than a nanosecond whereas the write access time is several nanoseconds. Therefore, the analytical model presented in this paper neglects the transient response of the cell junction and bitline capacitors. Thus, considering Figure 4, the expression for memristor current will be

$$i_w(t) = \frac{V_{DD}}{2(R_{ch} + R_{tg} + R_{BL} + R_m(t))} \tag{5}$$

This can be used with opposite signs to determine the time for both writing logic 0 (negative) and logic 1 (positive). Considering the window function in Equation (3) and the rate of change of state in Equation (2), the write logic 1 access time can be approximated as

$$T_w = \frac{R_{TOT} I_1 - R_{OFF} I_2}{\eta} \tag{6}$$

where $R_{TOT} = R_{ch} + R_{tg} + R_{BL} + R_{OFF}$, $\eta = \frac{V_{DD}\mu_v R_{ON}}{2L^2}$, I_1 and I_2 are the solutions to the integrals $\int_{0.1}^{0.9} \frac{1}{1-x^4}\,dx$ and $\int_{0.1}^{0.9} \frac{x}{1-x^4}\,dx$, respectively. Note that the resistance of the memristor in (1) is approximated as $R_m(t) \approx R_{OFF}(1 - x(t))$ for simplicity. The integrals are determined from the window function we considered previously to model the nonlinearity of the memristor at the boundaries in equation (3) with $p = 2$. For writing logic 0 into the cell, the same Equation (6), where I_1 and I_2 are the solutions to the integrals $\int_{0.1}^{0.9} \frac{1}{1-(x-1)^4}\,dx$ and $\int_{0.1}^{0.9} \frac{x}{1-(x-1)^4}\,dx$, respectively can be used. Considering the bitline capacitor transition time will lead to a complicated differential equation which does not have a closed-form solution. However, it can be solved numerically using MATLAB *ode* solvers. Therefore, the rate in state change of the memristor is the solution to

$$\frac{C_{BL} R_{OFF}(R_{tg} + R_{BL})(\frac{dx}{dt})^2}{\eta(1-x^4)} - \frac{(R_{TOT} - xR_{OFF})(\frac{dx}{dt})}{\eta(1-x^4)} + \frac{V_{DD}}{2} = 0 \tag{7}$$

where the first term includes the bitline capacitor transition time. A comparison of the write 1 access time of the 1T1R RRAM cell for different memristor thicknesses using analytical models and HSPICE simulations is illustrated in Figure 7. For the HSPICE simulations, the 32 nm CMOS predictive technology model (PTM) [17] is used for the transistor, while memristor is modeled based on the model in [6]. Here we considered write 1(0) access time as the time required for the memristor resistance to change between 10%

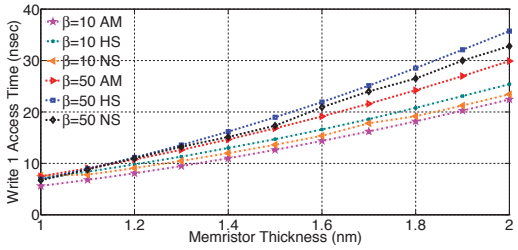

Figure 7: Analytical model vs HSPICE simulations for write 1 access time as a function of memristor thickness for different $\beta = \frac{R_{OFF}}{R_{ON}}$. AM = Analytical model ignoring bitline capacitance, HS = Hspice simulations and NS = Numerical solution accounting for bitline capacitance.

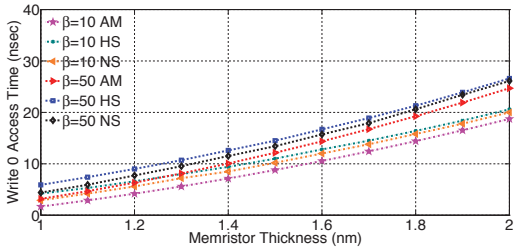

Figure 8: Analytical model vs HSPICE simulations for write 0 access time as a function of memristor thickness for different $\beta = \frac{R_{OFF}}{R_{ON}}$. AM = Analytical model ignoring bitline capacitance, HS = Hspice simulations and NS = Numerical solution accounting for bitline capacitance.

to 90% (90% to 10%) of $R_{OFF} - R_{ON}$ since the nonlinearity of the model at the borders leads to unacceptably large write access times. The proposed model underestimates the write access time by 15.1% average error as we neglected the transition times of the bitline and junction capacitors. Also it deviates from the HSPICE simulation for larger β values due to the increased nonlinearity of the device for larger R_{OFF}/R_{ON} ratios. Considering the capacitive transition times of the bitline will reduce the error to 7.3% based on the numerical solution of equation (7).

Similarly, Figure 8 shows the write 0 access time of the cell as function of the memristor thickness. The time to write logic 0 is less than the time to write 1 in the RRAM cell as the voltage drop (and hence the drive current) across memristor while writing 0 is $(V_{DD}/2)$ which is greater than that while writing logic 1 which is $(V_{DD} - V_{th} - V_{DD}/2)$ – due to the V_{th} across the pass transistor.

5.2 Read Operation Model

We define the read access time as the time required for the bitline to charge to $0.45V_{DD}$ while reading logic 0 (See Figure 9). If a cell with logic 1 stored in it were to be read out during this time, the bitline voltage will be larger than $V_{DD}/2$ (close to $0.65V_{DD}$ for this example). We use a differential sense amplifier with $V_{DD}/2$ and bitline voltage as two inputs to determine the data stored in the cell. As mentioned earlier, the sense amplifier has been designed to determine voltage differentials of 50 mV or larger. This approach is adopted as the memristor resistance does not change while reading 0, leading to a simplified read time model. The reading 1 process is destructive and results in the memristor state (i.e. memristance) changing during the read operation. Moreover, this change of state is nonlinear making it difficult to formulate a closed form expression. It

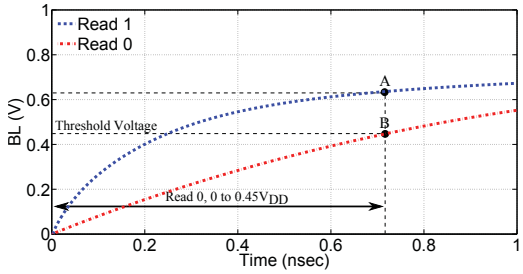

Figure 9: The read access time for 1T1R is defined as the time required for bitline voltage to increase from 0 V to $0.45V_{DD}$ while reading logic 0.

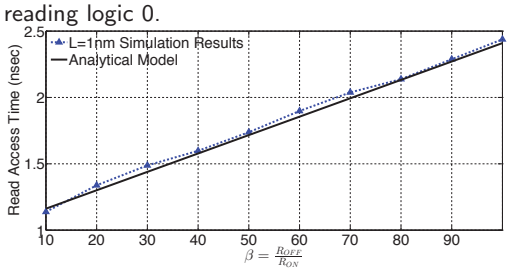

Figure 10: Analytical model versus HSPICE simulation results for read access time of the 1T1R cell as a function of β for different memristor thicknesses L. T_R is independent of memristor thickness ($R_{tg} = 582\Omega, R_{ON} = 100\Omega, C_{BL} = 200fF$).

should be noted that there is roughly 20% energy overhead with using read 0 for defining the read access time. This overhead can be decreased by using a threshold input lower than $V_{DD}/2$ to the sense amplifier.

To model the read access time, we consider the bitline voltage for the equivalent circuit in Figure 5. We need to consider the frequency response of the circuit as the read time is comparable to the charging/discharging time of C_{BL} and C_d. In order to analyze the frequency response of the bitline voltage, we use the KVL and KCL expressions which lead to the complete solution for the voltage on the bitline capacitor in Laplace domain as

$$V_{BL}(s) = \frac{1}{s(1 + 2\alpha s + \omega_0^2 s)} \tag{8}$$

where ω_0 and α are the natural frequency and the damping factor of any second order system, respectively. The time domain expression for the bitline voltage is

$$V_{BL}(t) = V_{DD} + Ae^{s_1 t} + Be^{s_2 t} \tag{9}$$

where s_1 and s_2 are the roots of the characteristic equation in (8). Considering $R_{tg} = 582\Omega, C_{BL} = 200fF, C_d = 3fF$, two poles are away by more than three orders of magnitude, and therefore the non-dominant pole can be neglected in the transient response of the cell while reading. In other words, C_{BL} is the dominant capacitor. Moreover, considering the Laplace inverse transform of the bitline voltage, we have $A \approx -1$ in Equation (9). Since the read access time of the 1T1R RRAM cell is smaller than the write access time, the transient response of the bitline capacitor cannot be neglected. In order to approximate the read access time from the time response of the cell in Equation (9), we use the method of open-circuit time constants in the high-frequency regime [18]. Neglecting (by making open-circuit) C_d, we can find the time constant associated to C_{BL}. Therefore, the final read access time can be approximated as

$$T_R = 0.69(R_{ch} + R_{BL} + R_{OFF})C_{BL}. \tag{10}$$

We show the read access time of the 1T1R cell in Figure 10 as a function of β values. It should be noted that

β	Refresh Energy	Refresh Time	Memristor Thickness	Refresh Energy	Refresh Time
10	172 fJ	3.04 ns	1.2 nm	172 fJ	3.58 ns
30	170 fJ	3.38 ns	1.4 nm	158 fJ	3.27 ns
50	170 fJ	3.74 ns	1.6 nm	132 fJ	2.52 ns
70	170 fJ	4.27 ns	1.8 nm	80 fJ	1.7 ns
90	170 fJ	4.91 ns	2 nm	24 fJ	0.48 ns

Table 1: Refresh time and energy dissipation of the 1T1R RRAM cell using HSPICE simulation for different β (left half) and memristor thickness (right half) values.

the read access time is a monotonically increasing function. The proposed model shows an acceptable matching with the HSPICE simulation results with an average error of 3.5%.

The 1T1R cell needs to be refreshed after every destructive read 1 cycle. The refresh cycle time can be modeled using the approach for write operation model. The refresh cycle time is however smaller than the write access time of the cell. The exact refresh cycle time depends on the destructiveness of the read operation and the physical properties of the memristor. Table 1 compares the refresh time and energy dissipation of the 1T1R RRAM cell using HSPICE simulation for different β and memristor thickness values.

6. ENERGY MODELS

In this section, we present the models for energy consumption during read and write operation. The proposed energy models can be used in the design exploration of a large memristive array architecture. It should be noted that the energy consumed in the word line, loadline and bitline is not explicitly included, but can be easily determined using $E = (C_{BL} + C_{LL} + C_{WL})V_{DD}^2$, where C_{BL}, C_{LL} and C_{WL} are the bitline, loadline and wordline capacitances.

6.1 Write Operation Model

As was mentioned in Section 5.1, the instantaneous current of the memristor while writing one or zero is determined by Equation (5), which depends on the memristor resistance at that instance of time. The energy dissipated in the cell can therefore be calculated as

$$E_W = \int_0^{T_W} \frac{V_{DD}}{2} i(t)\, dt = \frac{V_{DD}}{2\gamma} \int_{0.1}^{0.9} \frac{dx}{F(x)} = \frac{V_{DD} I_1}{2\gamma} \tag{11}$$

where $\gamma = \mu_v R_{ON}/L^2$ and $I_1 = \int_{0.1}^{0.9} \frac{1}{1-x^4}\, dx$ is the integral of the inverse of the window function. Also $V_{DD}/2$ is the series combination of the bitline charge voltage and the voltage at node LL (see Figure 4). According to (11), the energy dissipated in the 1T1R RRAM cell during write operation is a linear function of power supply and a quadratic function of the memristor thickness L. Moreover, the maximum memristor resistance i.e. R_{OFF} does not affect the dissipated energy. The same Equation (11) can be used for calculating the energy dissipated while writing logic 0, but with a different window function ($F(x) = 1 - (x-1)^4$) and boundary conditions (0.9 to 0.1).

Figure 11 shows the energy dissipated during write operation in a 1T1R RRAM cell as a function of memristor thickness for different values of β when calculated using analytical models and HSPICE simulations. There is an average error of 23.2% between the energy calculated using the proposed model neglecting the capacitive transition times while writing and HSPICE simulation. Using MATLAB *ode* solvers, we can numerically find the energy considering the capacitive transition times of the bitline which reduces the error to 11.3%. It should be noted that here dissipated energy

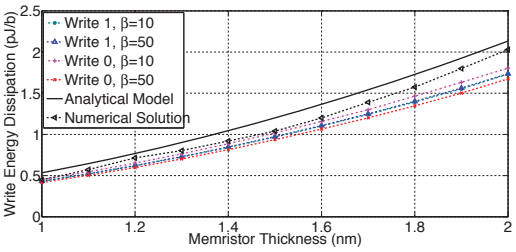

Figure 11: Analytical model versus HSPICE simulations for calculating the energy dissipated during write operation of a 1T1R RRAM cell as a function of memristor thickness for different β values ($R_{tg} = 582\Omega, R_{ON} = 100\Omega, C_{BL} = 200fF$). AM = Analytical model ignoring the bitline capacitance and NS = Numerical solution considering bitline capacitance.

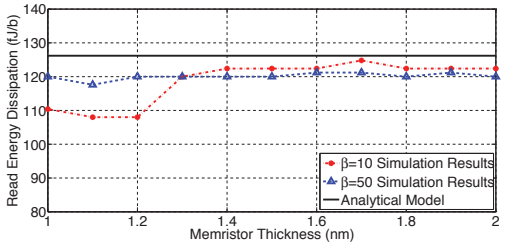

Figure 12: Read dissipated energy of the 1T1R cell as a function of memristor thickness for different β values. Read dissipated energy is independent of the memristor thickness and β ($R_{ON} = 100\Omega, C_{BL} = 200fF$).

corresponds to the required energy for the cell to change the state from 10% to 90% of its maximum value.

6.2 Read Operation Model

We propose the model for the energy dissipated while reading the 1T1R RRAM cell in this section. Using the equivalent circuit of the cell during read cycle (see Figure 5), the memristor current equation in time domain will be

$$i_R(t) = Ae^{s_1 t} + Be^{s_2 t}. \tag{12}$$

Similar to the read access time analysis, we can neglect the effects of the non-dominant pole. Therefore, the memristor current will simply be $i_R(t) \approx Ae^{s_1 t}$ where the coefficient $A = V_{DD}/(R_{ch} + R_{BL} + R_m(0))$, for reading one, $R_m(0) = R_{ON}$ and while reading zero, $R_m(0) = R_{OFF}$. The dissipated energy of the cell while reading can be expressed as

$$E_R = \int_0^{T_R} V_{DD} i_R(t)\, dt = \frac{V_{DD}^2}{(R_{ch} + R_{BL} + R_m(0))} \int_0^{T_R} e^{s_1 t}\, dt \tag{13}$$

where T_R is the read access time of the cell. Considering the dominant pole of the cell and the read access time equation in (10), the dissipated energy of the 1T1R RRAM cell is

$$E_R \approx 0.63 C_{BL} V_{DD}^2 \tag{14}$$

The read energy is therefore independent of the memristor physical parameters. A comparison of the read energy calculation using the proposed model and the HSPICE simulation is shown in Figure 12. The proposed model overestimates the dissipated energy since the open-circuit time constants method used in Equation (10) does not consider the non-dominant pole of the 1T1R cell leading to a larger cell current and energy. We can observe an average error of 6.5% between the model and the HSPICE simulation results.

7. CONCLUSION

In this paper, we derived accurate models for the performance and the energy dissipation of the 1T1R TiO_2-based RRAM cell. The models were verified against detailed HSPICE circuit simulations. The write access time is inversely proportional to minimum value of memristance and directly proportional to the square of memristor thickness. The read access time of the cell is only a function of the maximum value of memristance and does not change by the memrsitor thickness. Read operation is one order of magnitude faster than write operation in the 1T1R cell. From energy perspective, the write operation is roughly three times more energy consuming than the read operation. The write energy increases quadratically for larger memristor thicknesses while read energy dissipation depends only on the bitline capacitor and is not a function of the physical parameters of the memristor.

8. ACKNOWLEDGMENT

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