**EC571/Digital VLSI Circuit Design**
**Spring 2021**
Lecture: Mon-Wed 12:20 pm – 2:05 pm in PHO 211
Recitation/Lab: Friday 12:20 pm – 2:05 pm in PHO 307
Number of credits: 4, Prerequisites: EC 311, EK307, EC 410 (optional)

## Course Objective

The objective of this course is to learn how to design a digital CMOS circuits and digital VLSI systems for given area, power, performance, and reliability specifications.

## Staff Information

Instructor:
Ajay Joshi
Email: joshi@bu.edu **(Make sure you include EC571 in the subject line)**.
Office Hours: Tuesday and Thursday 5:30 pm ET to 6:30 pm ET via Zoom (link posted on Piazza).

Grader/Lab Assistant:
Timur Zirtiloglu
Email: timurz@bu.edu **(Make sure you include EC571 in the subject line)**.
Office Hours: Monday and Wednesday from 8 pm ET to 9 pm ET via Zoom (link posted on Piazza).

## Textbooks and Class Material

1. TextBook (strongly recommended): Digital Integrated Circuits - A Design Perspective, Second Edition. Rabaey et al., Prentice Hall. ISBN 0135974445.
2. TextBook (optional): Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, First Edition. Erik Brunvand, Addison-Wesley. ISBN 0321547993.
3. TextBook (optional): CMOS VLSI Design: A Circuits and Systems Perspective, Fourth Edition. Neil Weste, David Harris. ISBN 9780321547743.
4. Announcements, course material and other useful links will be posted on Blackboard (http://learn.bu.edu).
5. Piazza should be used for posting questions: (http://www.piazza.edu).
6. Gradescope will be used for submitting and grading homework (http://www.gradescope.edu).

## Course Goals

To provide students with:

1. Extensive training in the design of CMOS integrated circuits that perform an arbitrary digital function and meet an arbitrary performance specification.
2. Become proficient with a VLSI CAD tools.
3. Understanding of how to keep pace with the field as it crosses into "new territory" over the next few years.

**Course Outcomes**

As an outcome of completing this course, students should be able to:

1. Understand the MOSFET basics and their fabrication and the layout design rules.
2. Understand the operation of MOS transistor.
3. Understand the static characteristics of MOS inverters.
4. Design, implement and test: Inverter Sizing and Noise Margin Calculation.
5. Understand the switching characteristics and interconnect effects of MOS inverters.
6. Understand the implications of internal and external loading.
7. Design, implement and test: Buffer Chains used to drive big loads.
8. Understand Combinational MOS logic circuits.
9. Understand Sequential MOS logic circuits.
10. Understand Dynamic logic circuits.
11. Understand the working of ROM and RAM.
12. Understand limitations of the technology: Short channel effects.
13. Understand the use of chip I/O circuits.
14. Understand the design for manufacturability and testability.
15. Design, implement and test: Sequential circuits
16. Understand the fundamental concepts and technology implications of very short channel devices
17. Achieve proficiency with aspects of Cadence tool suite.

**Evaluation**

Grading

Two mid-term exams: 30% total (15% each), Final exam: 20%, Homeworks: 40% (5% per Homework), Project: 10%.

Exams

The mid-term exam will be during class time. The Final exam will be on TBD.

Project

We will do a group project at the end of the semester. Each group will consist for 2 students. Details of the project will be provided at a later date.

Homeworks

Homework assignments will consist of a pencil-paper component and/or a lab component. Homeworks are to be submitted before the beginning of the class on the date specified. You can discuss your work in abstract with other students in the class, but you should write-up the solutions on your own.

**Course Policies**

Pencil-Paper Component of the Homework:

The pencil-paper component of the homework assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions of homework problems by yourself. Copying the solution and/or answer from another student is considered cheating. Two identical homeworks with same mistakes are considered cheating. No extensions on homeworks will be provided.

Lab Component of the Homework:

The lab component of the homework assignments must be the result of your work. You can discuss your approach for completing the lab component with others, but not the detailed solution. Note that all lab components are to be submitted via github. We will compare each lab submission with other lab submissions. If we come across two solutions that are identical or closely match each other, then that will be considered cheating. No extensions on labs will be provided.

Makeup exams:

Makeup exams will be provided if the student takes prior permission from the instructor. Emergencies will be dealt on a case-by-case basis. Note that oversleeping, being not ready, overload due to projects or coursework in other classes are not valid excuses for requesting a makeup exam.

Exam/Home Grade discussion:

Grade discussion/corrections should be done within one week after the graded exam or homework is distributed. No grade changes will be made after one week, or after the last day of class.

I and W grades:

As per University policy.

Academic Integrity and Honor Code:

- Your submission of the homework assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions by yourself. Copying the solution and/or answer from another student or source is considered cheating.
- Clearly reference any sources you used in your work: books, Internet, and your collaborators!
- Boston University's academic code of conduct will be strictly applied.
- Boston University's computing ethics will be strictly applied.

**Course Schedule (subject to change)**

| Lecture Number | Date | Lecture Topic | Text Reference (Rabaey et al.) | Homework Due |
|---|---|---|---|---|
| 1 | Jan 25 | Introduction, MOS Manufacturing, Design rules | Chapter 1, 2 | |
| 2 | Jan 27 | CMOS Inverter Design and Analysis - I | Chapter 5 | |
| 3 | Feb 1 | CMOS Inverter Design and Analysis - II | Chapter 5 | |
| 4 | Feb 3 | Transistor Modeling - I | Chapter 3 | Hw 1 |
| 5 | Feb 8 | Transistor Modeling - II | Chapter 3 | |
| 6 | Feb 10 | Wire Modeling | Chapter 4 | Hw 2 |
| 7 | Feb 16 | Combinational Logic Gates - I | Chapter 6 | |
| 8 | Feb 17 | Combinational Logic Gates - II | Chapter 6 | Hw 3 |
| 9 | Feb 22 | Combinational Logic Gates - III | Chapter 6 | |
| 10 | Feb 24 | **Exam 1** | | |
| 11 | Mar 1 | Sequential Logic Circuits - I | Chapter 7 | |
| 12 | Mar 3 | Sequential Logic Circuits - II | Chapter 7 | |
| 13 | Mar 8 | Sequential Logic Circuits - III | Chapter 7 | Hw 4 |
| 14 | Mar 10 | Arithmetic Building Blocks - I | Chapter 11 | |
| 15 | Mar 15 | Arithmetic Building Blocks - II | Chapter 11 | Hw 5 |
| 16 | Mar 17 | Arithmetic Building Blocks - III | Chapter 11 | |
| 17 | Mar 22 | Memory - I | Chapter 12 | Hw 6 |
| 18 | Mar 24 | Memory - II | Chapter 12 | |
| 19 | Mar 29 | **Exam 2** | | |
| 20 | Mar 31 | Memory - III | Chapter 12 | |
| 21 | Apr 5 | Timing, Clock and Power - I | Chapter 10, 11 | |
| 22 | Apr 7 | Timing, Clock and Power - II | Chapter 10, 11 | Hw 7 |
| 23 | Apr 12 | Timing, Clock and Power - III | Chapter 10, 11 | |
| 24 | Apr 14 | Miscellaneous topics | | Hw 8 |
| 25 | Apr 19 | Miscellaneous topics | | |
| 26 | Apr 21 | Miscellaneous topics | | |
| 27 | Apr 26 | Project Presentations | | |
| 28 | Apr 28 | Project Presentations | | |
| | TBD | **Final Exam** | | |