

## EC513 – Computer Architecture

Spring 2017

Lecture: Tue-Thu 9 am – 10:45 am in CAS 237

Recitation/Lab: Friday 12:20 pm – 2:05 pm in PHO 305

Number of credits: 4, Prerequisites: EC 413, EC605 or equivalent

### Course Objective

The goal of this course is to learn the design of modern computer system architecture and develop a strong platform that could be leveraged to design future computer systems.

### Course Description

This course is a graduate course on computer architecture with an emphasis on a quantitative approach to cost/performance design tradeoffs. The course covers:

- Fundamentals of classical and modern processor design
- Evaluation metrics and trends, performance and cost issues
- ISAs (instruction set architectures)
- Datapath & pipelining (including branch prediction)
- Memory hierarchies, caches, & virtual memory (and virtual machines)
- Overview of semiconductor technology & energy/power
- Parallelism:
  - Instruction: out-of-order multiple issue, dynamic scheduling, speculation
  - Thread: multithreading, multicore, cache coherence and synchronization

### Staff Information

Instructor:

Name: Ajay J Joshi  
Office address: PHO 334  
Office phone number: 617-353-4840  
E-mail address: joshi@bu.edu (**Best way to contact me - Make sure you include EC513 in the subject line**)  
Office hours : PHO 334, 1 pm to 2 pm on Mon, 11 am to 12 noon on Fri or by appointment

Teaching Assistant/Lab Assistant:

Name: Marcia Sahaya Louis  
E-mail address: marcia93@bu.edu (**Make sure you include EC513 in the subject line**)  
Office hours : PHO 305, 10 am to 12 noon on Wed or by appointment

Name: Anmol Gupta  
E-mail address: apgupta10@bu.edu (**Make sure you include EC513 in the subject line**)  
Office hours : PHO 305, 1 pm to 3 pm on Tue and Thu or by appointment

Name: Shantanu Bobhate  
E-mail address: sbobhate@bu.edu (**Make sure you include EC513 in the subject line**)  
Office hours : PHO 305, 7 pm to 9 pm on Mon or by appointment

## Course Resources

- TextBook (strongly recommended): J. L. Hennessy and D. A. Patterson. **Computer Architecture: A Quantitative Approach**, 5th edition. Morgan Kaufmann, 2012 (ebook available from library).
- TextBook (optional): D.M. Harris and S.L. Harris. **Digital Design and Computer Architecture**, 2nd edition. Morgan Kaufmann, 2012.
- TextBook (optional): J. L. Patterson & D. A. Hennessy, **Computer Organization & Design: The Hardware/Software Interface**, 5th Edition, Morgan Kaufmann, 2013.
- Announcements, course material and other useful links: Will be posted on Blackboard (<http://learn.bu.edu>)
- Piazza (<https://piazza.com/bu/spring2017/ec513/home>) should be used for posting questions.

## Evaluation

Grading criterion:	One mid-term exam - 20% each, Final Exam – 20%, Labs - 40%, Homeworks - 20%.
Homework:	Homework assignments are to be submitted before the beginning of the class on the date specified. You can discuss your work in abstract with other students in the class, but you should write-up the solutions on your own.
Labs:	Lab assignments are to be submitted via github by the specified deadline. We will use Travis for checking your lab assignments. All lab assignments are to be done in a group. Groups should be formed by the end of first week of classes.
Exams:	There will be one mid-term exams and one final exam.

## Course Policy

- **Homework:** The homework assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions of homework problems by yourself. Copying the solution and/or answer from another student is considered cheating. Two identical homeworks with same mistakes are considered cheating. **No extensions on homeworks will be provided.**
- **Labs:** The lab assignments must be the result of your group's work. You can discuss your approach for completing the lab assignments with other groups, but not the detailed solution. Note that all lab assignments are to be submitted via github and will be checked using Travis. We will compare each group's lab submission with other lab submissions. If we come across two solutions that are identical or closely match each other, then that will be considered cheating. **No extensions on labs will be provided.**
- **Makeup exams:** Makeup exams will be provided if the student takes prior permission from the instructor. Emergencies will be dealt on a case-by-case basis. Note that oversleeping, being not ready, overload due to projects or coursework in other classes **are not valid excuses** for requesting a makeup exam.
- **Exam/Home Grade discussion:** Grade discussion/corrections should be done within one week after the graded exam or homework is distributed. No grade changes will be made after one week, or after the last day of class.
- **I and W grades:** As per University policy.
- **Honor Code:** If you are found cheating on homeworks, labs or examinations, you will be brought up on charges before the **Student Academic Conduct Committee** whose punishment may include suspension from the University without the right to transfer credits for courses.

**Schedule for EC513 - Lectures, Homeworks, Labs and Exams (subject to change)**

<b>Schedule for EC513 - Lectures, Homeworks, Labs and Exams (subject to change)</b>							
<b>Lec #</b>	<b>Date</b>	<b>Topic</b>	<b>Text Ref</b>	<b>Hw Out</b>	<b>Hw Due</b>	<b>Lab Out</b>	<b>Lab Due</b>
1	1/19	Introduction					
2	1/24	Technology trends					
3	1/26	Technology trends				Lab1	
4	1/31	Performance		Hw1			
5	2/2	ISAs					
6	2/7	ISAs			Hw1		
7	2/9	Pipelining				Lab2	Lab1
8	2/14	Pipelining hazards		Hw2			
9	2/16	Pipelining hazards, branch prediction					
10	2/23	Branch prediction			Hw2		
11	2/28	Caching					
12	3/2	<b>Mid-term Exam</b>					
13	3/14	Caching					
14	3/16	Caching		Hw3			
15	3/21	Caching				Lab3	Lab2
16	3/23	Virtual memory			Hw3		
17	3/28	Virtual memory					
18	3/30	Superscalar		Hw4			
19	4/4	Static scheduling					
20	4/6	Dynamic scheduling			Hw4		
21	4/11	Dynamic scheduling				Lab4	Lab3
22	4/13	Network microarchitecture		Hw5			
23	4/18	Network microarchitecture					
24	4/20	Network microarchitecture			Hw5		
25	4/25	Multicore					
26	4/27	Multicore					
27	5/2	Miscellaneous topics					Lab4
28	TBD	<b>Final Exam</b>					