EC311 - Introduction to Logic Design
Spring 2012

Class: MW 12 noon - 2 pm in PHO 210
Lab: Section B1, Tue 6 pm - 8 pm in PHO 115
Section B2, Tue 10 am - 12 noon in PHO 115
Section B3, Thu 6 pm - 8 pm in PHO 115
Section B4, Tue 2 pm - 4 pm in PHO 115
Number of credits: 4

Course objectives

The class covers the theory and practice of digital hardware design. Students will learn to formulate real world tasks using Boolean algebra and FSM theory, and to apply manual and computer-aided techniques to solve the problems. In addition, they will also learn fundamental circuit design and verification skills using Verilog HDL and FPGAs.

Staff Information

Instructor:

Name:	Ajay J Joshi
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Office phone number:	617-353-4840
E-mail address:	joshi@bu.edu (**Best way to contact me - Include EC311 in the subject line**)
Office hours :	PHO 334, Tue 5 pm - 6 pm, Fri 11 am - 12 noon or by appointment

Graduate Teaching Fellow:

Name:	Fulya Kaplan
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Office hours :	PHO 115, Mon 3 pm - 4 pm or by appointment

Lab Assistant:

Name:	Alice Tsing
E-mail address:	atsing@bu.edu (**Include EC311 in the subject line**)
Office hours :	PHO 115, Thu 5 pm - 6 pm or by appointment

Course Resources

TextBooks :

1. **Digital Design,** Second Edition, Frank Vahid, Wiley. ISBN 978-0-470-53108-2
2. **Verilog for Digital Design**, Frank Vahid and Roman Lysecky, Wiley. ISBN 978-0-470-05262-4

Announcements, course material and other useful links:

Will be posted on Blackboard (http://blackboard.bu.edu)

Goals

To provide students with:

- An understanding of the basic tools of logic design
- An understanding of sound design methodologies
- An experience with hardware implementation and the use of CAD tools

Course Outcomes

As an outcome of completing this course, students should be able to:

- Understand the applications of logic design
- Understand abstraction and hierarchy in digital design
- Understand what components are available for logic design
- Understand the use of Boolean algebra in logic analysis and design
- Understand logic minimization criteria and methods for use in design
- Understand the concept of state in digital systems
- Design combinational digital logic systems given specifications
- Design sequential digital logic systems (finite state machines) given specifications
- Implement logic designs in hardware and with CAD tools
- Discover component availability and data using the Internet or other resources
- Write brief reports on assigned topics

Evaluation

Grading:	Two Midterms - 15% each, Final Exam - 20%, Project - 14%, Labs - 12%, Homework - 24%. Class Participation will help your grade.
Homework:	Homework assignments will be posted on the Blackboard website one week ahead of their due dates. Homeworks are to be submitted before the beginning of the class on the date specified. You can discuss your work in abstract with other students in the class, but you should write-up the solutions on your own.
Labs:	Lab descriptions will be posted on the Blackboard website. You should have a bound lab notebook of standard page format. All required paperwork (truth tables, K-maps, logic diagram and circuit layout showing pin connections) for the lab must be in your lab notebook. Labs will be given a "Complete/Incomplete" grade.
Exams:	There will be two mid-term exams and a final exam.
Project:	Work as a team of 3 students. Project presentations will be during the last week of classes (see schedule). Project presentation will be done in front of all students, and so should be treated as professional presentations.

Course Policy

- **Homework/Lab**: The homework assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions of HW/Lab problems by yourself. Copying the solution and/or answer from another student is considered cheating. Two identical HWs/Labs with same mistakes are considered cheating. **No extensions on homeworks or labs will be provided.**

- **Makeup exams**: Makeup exams will be provided if the students takes prior permission from the instructor. Emergencies will be dealt on a case-by-case basis. Note that oversleeping, being not ready, overload due to projects or coursework in other classes **are not valid excuses** for requesting a makeup exam.
- **Exam/Home/Lab Grade discussion**: Grade discussion/corrections should be done within one week after the graded exam of homework is distributed. No grade changes will be made after one week, or after the last day of class.
- **I and W grades**: As per University policy.
- **Honor Code**: If you are found cheating on HWs, Labs, or examinations, you will be brought up on charges before the **Student Academic Conduct Committee** whose punishment may include suspension from the University without the right to transfer credits for courses taken elsewhere.

Schedule for EC311 - Lectures, Homeworks, Labs and Exams

Lec #	Date	Topic Description	Labs	Hw Out	Hw Due
1	1/18	Introduction, What is logic design? Switches as basis for digital computation, CMOS technology: transistors and gates			
2	1/23	Number systems and codes, Combinational vs. sequential systems		Hw 1	
3	1/25	Combinational logic, Boolean algebra			
4	1/30	Canonical forms, Algebraic simplification, Logical minimization. Boolean cubes	Prelab	Hw 2	Hw 1
5	2/1	Karnaugh maps			
6	2/6	Verilog Introduction	Lab 1	Hw 3	Hw 2
7	2/8	FPGA design			
8	2/13	Map manipulation, Prime implicants Multilevel logic	Lab 2	Hw 4	Hw 3
9	2/15	Delay, Timing Waveform, Hazards, Glitches, Multiplexers and demultiplexers			
10	2/21	Review for Mid-term 1			Hw 4
11	2/22	Midterm 1			

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12	2/27	Multiplexers as general-purpose logic functions, Gate array, Look-up tables, PLA's,	Lab 3		
13	2/29	Two's Complement, Adder Design, Multiplier		Hw 5	
14	3/5	Sequential logic, Latches, Flip-flops	Lab 4		
15	3/7	Sequential Components, Registers. Metastability		Hw 6	Hw 5
Spring Break					
16	3/19	Counters	Lab 5		
17	3/21	Finite State Machine, FSM Design Approach	Project	Hw 7	Hw 6
18	3/26	Optimization of FSM	Lab 6		
19	3/28	RTL Design, State Encoding, Traffic Controller		Hw 8	Hw 7
20	4/2	Implementation examples, Specification of State Diagram			
21	4/4	Review for Midterm 2			Hw 8
22	4/9	Midterm 2			
23	4/11	Memory	Project review		
24	4/18	Computer organization, Processors			
25	4/23	Course review			
26	4/25	Project presentations			
27	4/30	Project presentations			
28	5/2	Project presentations			
	TBD	Final exam			