EC311/Introduction to Logic Design
Fall 2019

Class: MW 12:20 pm to 2:05 pm in PHO 203

Course Objective

The class covers the theory and practice of digital hardware design. Students will learn to formulate real world tasks using Boolean algebra and FSM theory, and to apply manual and computer-aided techniques to solve the problems. In addition, they will also learn fundamental logic design and verification skills using Verilog HDL and FPGAs.

Staff Information

Instructor:
Ajay Joshi
Email: joshi@bu.edu (Include EC311 in the subject line).
Office Hours: Friday 3:00 pm to 4 pm or by appointment in PHO 334.

GTFs:
Zahra Azad
Email: zazad@bu.edu (Include EC311 in the subject line).
Office Hours: Wednesday 7:30 pm to 8:30 pm or by appointment in PHO 115.

Rashmi Agarwal
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Office Hours: Thursday 12:30 pm to 1:30 pm or by appointment in PHO 115.

Marcia Sahaya Louis
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Office Hours: Tuesday 12:30 pm to 1:30 pmor by appointment in PHO 115.

UTFs
Pallavi Balivada (pallavib@bu.edu)
Zachary Bachrach (bachrach@bu.edu)
Quinn Meurer (quinnyyy@bu.edu)

Textbooks and Class Material

Digital Design, Sixth Edition, Mano and Ciletti, Pearson (5th edition is also acceptable).
Starter's Guide to Verilog 2001, Ciletti. Pearson.

Assignments, announcements, course material, updated schedule, and other useful links will be posted on Blackboard (http://learn.bu.edu) and/or Piazza (https://piazza.com/). Please use Piazza for asking questions.

Course Goals

To provide students with:

- An experience with digital logic implementation.

- An understanding of the CAD tools used for logic design.
- An understanding of sound logic design methodologies.

Course Outcomes
As an outcome of completing this course, students should be able to:

- Understand the applications of logic design
- Understand abstraction and hierarchy in digital design
- Understand what components are available for logic design
- Understand the use of Boolean algebra in logic analysis and design
- Understand logic minimization criteria and methods for use in design
- Understand the concept of state in digital systems
- Design combinational digital logic systems given specifications
- Design sequential digital logic systems (finite state machines) given specifications
- Implement logic designs in hardware and with CAD tools
- Discover component availability and data using the Internet or other resources

Evaluation
Grading
Two in-class exams: 15% each, One final exam: 25%, Project: 14%, Labs: 15%, Homework: 16%.

Exams
The first two exams will be during class time. The third exam will take place during the scheduled final exam timeslot.

Project
We will do a group project at the end of the semester. Each group will consist for 4-5 students. Details of the project will be provided at a later date.

Labs
Lab assignments will be posted on the Blackboard website. Grades will be assigned to completed labs. Students are expected to attend their scheduled lab section every week.

Homeworks
Homework assignments will be posted on the Blackboard website. Homeworks are to be submitted before the specified deadline. No credit will be given for late homework

Course Policies
Exam/Homework/Lab Grade discussion:
Grade discussion/corrections should be done within one week after the graded exam or homework is distributed. No grade changes will be made after one week.

Academic integrity:

- The homework and lab assignments must be the result of your individual work. You may discuss the contents and general approach to a problem with your classmates but not the detailed solution. You are expected to formulate your approach and write the solutions of Homework/Lab problems by yourself. Copying the solution and/or answer from another student or source is considered cheating.
- Clearly reference any sources you used in your work: books, Internet, and your collaborators!
- Boston University's academic code of conduct will be strictly applied.
- Boston University's computing ethics will be strictly applied.

Course Schedule

Lecture Number	Date	Lecture Topic	Reading Chapters (Mano)	Homework Due	Lab Due
1	Sep 4	Introduction	1.1-1.6		
2	Sep 9	Numbers, codes, binary arithmetic, gates	1.6-2.0		
3	Sep 11	Boolean algebra, canonical forms	2.0-2.8		
4	Sep 16	K-Maps, Logic minimization, PI's	3.1-3.5	Hw 1	Lab A
5	Sep 18	Gate implementation	3.6-3.8		
6	Sep 23	Verilog: Alternative ways to describe a circuit	3.9	Hw 2	Lab B
7	Sep 25	Combinational logic	4.1-4.5		
8	Sep 30	Adders, multipliers, comparators	4.5-4.8	Hw 3	
9	Oct 2	Decoder, encoders	4.9-4.10		
10	Oct 7	Encoders, MUXes	4.10-4.11	Hw 4	
11	Oct 9	MUXes, tri-state	4.10-4.12		Lab 1
12	Oct 15	Synchronous sequential logic: latches and FFs Exam 1 review	5.1-5.4		
13	Oct 16	**Exam 1**			
14	Oct 21	Synchronous sequentail logic: state machines	5.5-5.7		

Lecture Number	Date	Lecture Topic	Reading Chapters (Mano)	Homework Due	Lab Due
15	Oct 23	State assignment, synthesis - cont	5.7-5.8		
16	Oct 28	State machines - cont	5.7-5.8	Hw 5	
17	Oct 30	Registers	6.1-6.3		
18	Nov 4	Counters,	6.4-6.6	Hw 6	
19	Nov 6	Memory	7.1-7.2		
20	Nov 11	Error codes	7.3-7.4	Hw 7	
21	Nov 13	ROM, PLD, PLA, PAL	7.5-7.7		
22	Nov 18	PAL, Xilinx architecture	7.7-7.8	Hw 8	
23	Nov 20	Exam 2 review			Lab 2
24	Nov 25	**Exam 2**			
25	Dec 2	Xilinx architecture, VLSI intro			
26	Dec 4	Review			
27	Dec 9	Project presentation			
28	Dec 11	Project presentation			
	TBD	**Final Exam**			