ColdFire

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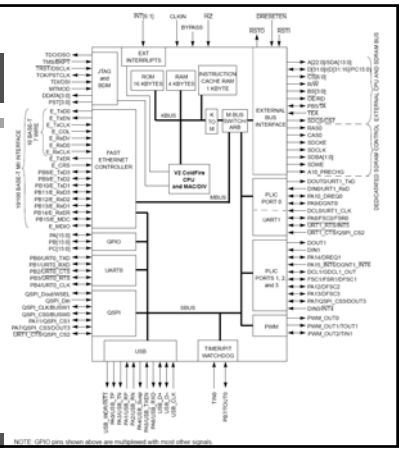
Overview

- **The MCF5272 ColdFire is a 32-bit, 66 MHz processor based on the Version 2 ColdFire Core**
- **4K Internal SRAM**
- **16K Internal ROM**
- **1K Instruction Cache**
- **Fully static operation with stop and sleep mode**
- **Individual module clock enables**
- **Very rapid response times to Interrupts from low power and sleep modes**
- **Software-controlled disable of external clock input for virtually zero power consumption**
- **Operating voltage of 3.3 v**

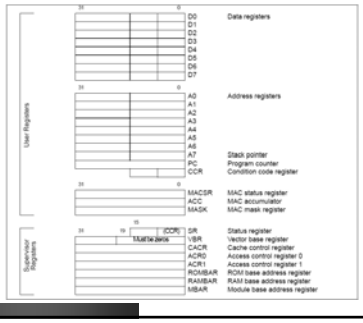
Peripherals

- **IEEE 802.3 compliant 10/100 Fast Ethernet Controller (FEC), with dedicated DMA**
- **USB 1.1 device controller and transceiver**
- **4 TDM ports**
- **PLIC module – Intended for ISDN designs**
- **QSPI – 16 stacked transfers**
- **SDRAM controller**
- **3 PWM outputs**
- **2 UARTs – baud rates up to 5 Mbps**
- **1-channel DMA**
- **8 chip selects**
- **16-bit general purpose I/Os**
- **4 16-bit timers and SW watchdog timer**

Block Diagram



Programming Model



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Programming Model

- **16 general purpose 32-bit registers, A0-A7 and D0-D7**
- **32-bit Program Counter**
- **8-bit Condition Code Register**
- **Data registers can be accessed as 8, 16, or 32 bit values and can be used as index registers**
- **A0-A6 can be used as software stack pointers, index registers, or base address registers**
- **A7 is the system Stack Pointer**

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Condition Code Register

- **Bits 7:5 are reserved and should always be written to 0**
- **X – Assigns the value of a carry bit**
- **N – Negative flag**
- **Z – Zero condition code bit**
- **V – Overflow condition code bit**
- **C – Carry condition code bit**

	7	6	5	4	3	2	1	0
Field	—			X	N	Z	V	C
Reset	000			Undefined				
R/W	R			R/W	R/W	R/W	R/W	R/W

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Supervisor Programming Model

- **Supervisor functions, performed by the MOVEC instruction, enable programmers to implement Operating System functions such as memory and I/O control.**
- **It enables configuring CPU attributes such as cache enable**

Rc[11–0]	Register Definition
0x002	Cache control register (CACR)
0x004	Access control register 0 (ACR0)
0x005	Access control register 1 (ACR1)
0x801	Vector base register (VBR)
0xC00	ROM base address register
0xC04	RAM base address register (RAMBAR)
0xC0F	Module base address register (MBAR)

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The Status Register SR

- **The SR register provides processor status, interrupt priority mask, and other control bits.**
- **The Supervisor can read/write the entire SR register, but the user is limited to read/write of SR[7:0]**

	15					8	7					0
	System Byte						Condition Code Register (CCR)					
Field	T	—	S	M	—	I	—	X	N	Z	V	C
Reset	0	0	1	0	0	111	000	—	—	—	—	—
R/W	R/W	R	R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W

- **T – Trace enable**
- **S – Supervisor vs. User state**
- **M – Master Interrupt State**
- **I – Interrupt Priority Mask**

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Vector Base Address Register

- **The VBR is an address register which indicates where in memory the processor vector table is stored**
- **The ColdFire processor supports a 1024 vector table aligned on any 1 MB address boundary**
- **The Vector table contains 256 entries, the first 64 of which are defined by Motorola and the remaining 192 are user defined vector addresses**

	31 … 20	19 … 0
Field	Exception vector table base address	—
Reset	0000_0000_0000_0000_0000_0000_0000_0000	
R/W	Written from a BDM serial command or from the CPU using the MOVEC instruction. VBR can be read from the debug module only. The upper 12 bits are returned, the low-order 20 bits are undefined.	
Rc[11–0]	0x801	

Figure 2-6. Vector Base Register (VBR)

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Exception Processing

Vector Numbers	Vector Offset (Hex)	Stacked Program Counter [1]	Assignment
0	000	—	Initial stack pointer
1	004	—	Initial program counter
2	008	Fault	Access error
3	00C	Fault	Address error
4	010	Fault	Illegal instruction
5	014	Fault	Divide by zero
6–7	018–01C	—	Reserved
8	020	Fault	Privilege violation
9	024	Next	Trace
10	028	Fault	Unimplemented line-a opcode
11	02C	Fault	Unimplemented line-f opcode
12	030	Next	Debug interrupt
13	034	—	Reserved
14	038	Fault	Format error
15	03C	Next	Uninitialized interrupt
16–23	040–05C	—	Reserved
24	060	Next	Spurious interrupt
25–31	064–07C	Next	Level 1–7 autovectored interrupts
32–47	080–0BC	Next	Trap #0–15 instructions
48–60	0C0–0F0	—	Reserved
61	0F4	Fault	Unsupported instruction
62–63	0F8–0FC	—	Reserved
64–255	100–3FC	Next	User-defined interrupts

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Exception Processing

- **The ColdFire processor inhibits interrupts during the first instruction of all exception handlers**
- **This enables the programmer to disable interrupts by raising the interrupt mask level in the status register**
- **There are many sources for exception, however the following usually indicate a fatal error:**

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Exceptions

- **Access Error**
  - **Caused by an error when accessing memory**
- **Address Error**
  - **Caused by addressing an odd instruction address (bit 0 of address is set)**
- **Illegal Instruction**
  - **Executing illegal opcodes such as 0x0000 and 0x4AFC**
- **Divide by Zero**
- **Privilege Violation**
  - **Attempted execution of a supervisor mode when in user mode**

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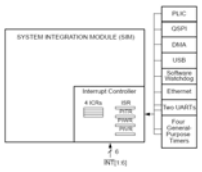
Interrupts

- **There are four interrupt control registers ICR1-4, which are used to assign interrupt levels to interrupt sources**
- **The ISR register allows for reading the instantaneous values of an interrupt source**
- **The PITR specifies transition level of interrupt**



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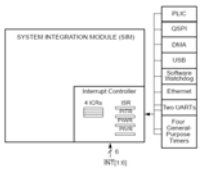
Interrupts

- **The PIWR specifies which interrupts can bring the CPU out of sleep mode**
- **The PIVR specifies which vector number is returned in response to an interrupt acknowledge cycle**
- **Interrupt Priorities are set through IPL, but if they all have the same IPL, priority is established through:**



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Interrupt Priority

Mnemonic or Portion Thereof	Description
INT1, INT2, INT3, INT4, INT5, INT6	External interrupt signals 1–6.
TMR0, TMR1, TMR2, TMR3	Timers 3–0 from timer module
USB0, USB1, USB2, USB3, USB4, USB5, USB6, USB7	USB endpoint 0–7
UART1, UART2	UART1, UART2 modules
PLIP	PLIC 2-KHz periodic interrupt, 2B+D data
PLIA	PLIC asynchronous and maintenance channels interrupt
DMA	DMA controller interrupt

Mnemonic or Portion Thereof	Description
ETx	Ethernet module transmit data interrupt
ERx	Ethernet module receive data interrupt
ENTC	Ethernet module non-time-critical interrupt
QSPI	Queued serial peripheral interface
IPL2, IPL1, IPL0	Interrupt priority level bits 2–0
PI	Pending interrupt
PDN	Power down enable
WK	Wakeup enable
SWTO	Software watchdog timer time out

Interrupt Controller Registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x020	Interrupt control register 1 (ICR1) [p. 7-4]			
0x024	Interrupt control register 2 (ICR2) [p. 7-5]			
0x028	Interrupt control register 3 (ICR3) [p. 7-5]			
0x02C	Interrupt control register 4 (ICR4) [p. 7-6]			
0x030	Interrupt source register (ISR) [p. 7-6]			
0x034	Programmable interrupt transition register (PITR) [p. 7-7]			
0x038	Programmable interrupt wakeup register (PIWR) [p. 7-8]			
0x03C	Reserved			Programmable interrupt vector register (PIVR) [p. 7-8]

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Interrupt Control Register ICR1

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	INT1PI	INT1IPL			INT2PI	INT2IPL			INT3PI	INT3IPL			INT4PI	INT4IPL		
Reset	0000_0000_0000_0000															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	TMR0PI	TMR0IPL			TMR1PI	TMR1IPL			TMR2PI	TMR2IPL			TMR3PI	TMR3IPL		
Reset	0000_0000_0000_0000															
R/W	R/W															
Addr	MBAR + 0x020															

Bits	Name	Description
31, 27, 23, 19, 15, 11, 7, 3	PI	Pending interrupt. Writing a 1 enables the value for the corresponding IPL field to be set. Note: for external interrupts only, writing a one to this bit clears the corresponding interrupt latch. The external interrupt must be toggled before another interrupt is latched. For all on-chip interrupt sources, this bit is cleared when the interrupt is cleared in the module registers. 0 No interrupt pending 1 An interrupt is pending.
30–28, 26–24, 22–20, 18–16, 14–12, 10–8, 6–4, 2–0	IPL	Interrupt priority level. Specifies the IPL for the corresponding interrupt source. This field can be changed only when a 1 is simultaneously written to the corresponding PI bit. 000 The corresponding $\overline{INT}$ source is inhibited and cannot generate interrupts. The state of the signal can still be read in the ISR. 001–111The corresponding $\overline{INT}$ source is enabled and generates an interrupt with the indicated priority level.

ICR2

	31	30	28	27	26	24	23	22	20	19	18	16
Field	UART1PI	UART1IIPL		UART2PI	UART2IIPL		PLIPPI	PLIPIPL		PLIAPI	PLIAIPL	
Reset	0000_0000_0000_0000											

	15	14	12	11	10	8	7	6	4	3	2	0
Field	USB0PI	USB0IIPL		USB1PI	USB1IIPL		USB2PI	USB2IPL		USB3PI	USB3IIPL	
Reset	0000_0000_0000_0000											
R/W	R/W											
Addr	MBAR + 0x024											

Figure 7-3. Interrupt Control Register 2 (ICR2)

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ICR3

	31	30	28	27	26	24	23	22	20	19	18	16
Field	USB4PI	USB4IIPL		USB5PI	USB5IIPL		USB6PI	USB6IIPL		USB7PI	USB7IIPL	
Reset	0000_0000_0000_0000											

	15	14	12	11	10	8	7	6	4	3	2	0
Field	DMAIPI	DMAIIPL		ERXPI	ERXIIPL		ETXPI	ETXIIPL		ENTCPI	ENTCIPL	
Reset	0000_0000_0000_0000											
R/W	R/W											
Addr	MBAR + 0x028											

Figure 7-4. Interrupt Control Register 3 (ICR3)

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ICR4

	31	30	28	27	26	24	23	22	20	19	18	16
Field	QSPIIPI	QSPIIIPL		INT5PI	INT5IIPL		INT6PI	INT6IIPL		SWTOIPI	SWTOIIPL	
Reset	0000_0000_0000_0000											

	15	0
Field	—	
Reset	0000_0000_0000_0000	
R/W	R/W	
Addr	MBAR + 0x02C	

Figure 7-5. Interrupt Control Register 4(ICR4)

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Interrupt Vector Table

Vector Number	Bits 4–0	Source	Function
64	00000	Reserved	User Spurious Interrupt
65	00001	INT1	External Interrupt Input 1
66	00010	INT2	External Interrupt Input 2
67	00011	INT3	External Interrupt Input 3
68	00100	INT4	External Interrupt Input 4
69	00101	TMR0	Timer 0
70	00110	TMR1	Timer 1
71	00111	TMR2	Timer 2
72	01000	TMR3	Timer 3
73	01001	UART1	UART 1
74	01010	UART2	UART 2
75	01011	PLIP	PLIC 2KHz Periodic

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Interrupt Vector Table

Vector Number	Bits 4–0	Source	Function
76	01100	PLIA	PLIC Asynchronous
77	01101	USB0	USB Endpoint 0
78	01110	USB1	USB Endpoint 1
79	01111	USB2	USB Endpoint 2
80	10000	USB3	USB Endpoint 3
81	10001	USB4	USB Endpoint 4
82	10010	USB5	USB Endpoint 5
83	10011	USB6	USB Endpoint 6
84	10100	USB7	USB Endpoint 7
85	10101	DMA	DMA Controller
86	10110	ERx	Ethernet Receiver
87	10111	ETx	Ethernet Transmitter
88	11000	ENTC	Ethernet Module Non-time-critical
89	11001	QSPI	Queued Serial Peripheral Interface
90	11010	INT5	External Interrupt Input 5
91	11011	INT6	External Interrupt Input 6
92	11100	SWTO	Software Watchdog Timer Timeout
93	11101	Reserved	Reserved
94	11110	Reserved	Reserved
95	11111	Reserved	Reserved

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Power Management

- **In *sleep mode* the processor allows any interrupt condition to wake up the processor**
- **Because it is a static design, sleep mode simply disables the clock to the processor's modules. When an interrupt occurs, execution is simply resumed from the point where the processor was placed into sleep mode**
- ***Stop mode* is achieved by setting a bit in the control register, which disables both the core and the peripherals.**
- **In stop mode, the processor consumes very little power and is brought out of the stop mode through an external interrupt event.**

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Local Memory - SRAM

- **The MCF5272 provides a local memory with the following parameters**
  - **4K SRAM organized as 1K x 32 bits**
  - **Sing-cycle access**
  - **Programmable base address**
  - **Ideal for use as system stack, or for storing critical code or data**

Address (using MOVEC)	Name	Width	Description	Reset Value
0x002	CACR	32	Cache control register	0x0000
0x004	ACR0	32	Access control register 0	0x0000
0x005	ACR1	32	Access control register 1	0x0000
0xC00	ROMBAR	32	ROM base address register	Uninitialized (except V = 0)
0xC04	RAMBAR	32	SRAM base address register	Uninitialized (except V = 0)

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MBAR

- **The supervisor-level MBAR register provides a base address for the internal peripherals**
- **The MBAR[V] bit is cleared by the system at reset time in order to prevent incorrect references before MBAR is set**
- **All internal peripheral registers occupy a single relocatable memory block along 64K boundaries**

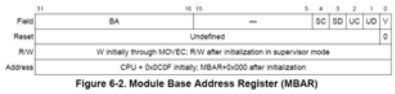

Figure 6-2. Module Base Address Register (MBAR)

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MBAR

Bits	Field	Description
31–16	BA	Base address. Defines the base address for a 64-Kbyte address range.
15–5	—	Reserved, should be cleared.
4	SC	Setting masks supervisor code space in MBAR address range
3	SD	Setting masks supervisor data space in MBAR address range
2	UC	Setting masks user code space in MBAR address range
1	UD	Setting masks user data space in MBAR address range
0	V	Valid. Determines whether MBAR settings are valid. 0 MBAR contents are invalid. 1 MBAR contents are valid.

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RAMBAR

- **The SRAM Base Address Register (RAMBAR) determines the address of the internal SRAM as well as other parameters:**

	31 … 12	11 … 9	8	7	6	5	4	3	2	1	0
Field	BA	—	WP	—	C/I	SC	SD	UC	UD	V	
Reset	—									0	
R/W	W for CPU; R/W for debug										
Address	CPU space + 0xC04										

Bits	Name	Description
31–12	BA	Base address. SRAM module base address. The SRAM module occupies a 4-Kbyte space defined by BA. SRAM can reside on any 4-Kbyte boundary in the 4-Gbyte address space.
11–9	—	Reserved, should be cleared.
8	WP	Write protect. Controls read/write properties of the SRAM. 0 Allows read and write accesses to the SRAM module. 1 Allows only read accesses to the SRAM module. Any attempted write reference generates an access error exception to the ColdFire processor core.
7–6	—	Reserved, should be cleared.

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RAMBAR

Bits	Name	Description
5–1	C/I, SC, SD, UC, UD	Address space masks (ASn). These fields allow certain types of accesses to be masked, or inhibited from accessing the SRAM module. These bits are useful for power management as described in Section 4.3.2.3, "Programming RAMBAR for Power Management." In particular, C/I is typically set. The address space mask bits are follows: C/I = CPU space/interrupt acknowledge cycle mask. Note that C/I must be set if BA = 0. SC = Supervisor code address space mask SD = Supervisor data address space mask UC = User code address space mask UD = User data address space mask For each ASn bit: 0 An access to the SRAM module can occur for this address space 1 Disable this address space from the SRAM module. References to this address space cannot access the SRAM module and are processed like other non-SRAM references.
0	V	Valid. Enables/disables the SRAM module. V is cleared at reset. 0 RAMBAR contents are not valid. 1 RAMBAR contents are valid.

- **After reset, the contents of SRAM are undefined and needs to be initialized before use**

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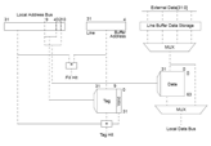
Instruction Cache

- **1 K direct-mapped cache**
- **Single-cycle access on cache hits**
- **16 byte line-fill buffer**
- **Organized as 64 lines of 16 bytes, and consists of a 64-entry tag array**
- **CACR[CINVA] forces the entire cache to be marked as invalid**
- **CPUSHL can invalidate a single cache line**
- **Reset clears the CACR and disables the instruction cache**



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Cache Programming Model

Address (using MOVEC)	Name	Width	Description	Reset Value
0x002	CACR	32	Cache control register	0x0000
0x004	ACR0	32	Access control register 0	0x0000
0x005	ACR1	32	Access control register 1	0x0000

	31	30	29	28	27	26	25	24	23	16
Field	CENB	—		CDPI	CFRZ	—		CINVA	—	
Reset	0000_0000_0000_0000									
R/W	Write (R/W by debug module)									

	15	10	9	8	7	6	5	4	2	1	0
Field	—	CEIB	DCM	DBWE	—	DWP	—				CLNF
Reset	0000_0000_0000_0000										
R/W	Write (R/W by debug module)										
Rc	0x002										

Figure 4-4. Cache Control Register (CACR)

Cache Programming Model

Bits	Name	Description
31	CENB	Enable cache. 0 Cache disabled. The cache is not operational; but data and tags are preserved. 1 Cache enabled.
30–29	—	Reserved, should be cleared.
28	CDPI	Disable CPUSHL invalidation. 0 Cache disabled 1 Cache enabled

Bits	Name	Description
1–0	CLNF	Control long-word fetch. Controls the size of the memory request the cache issues to the bus controller for different initial line access offsets.

CLNF	Longword Address Bits			
	00	01	10	11
00	Line	Line	Line	Long-word
01	Line	Line	Long-word	Long-word
1x	Line	Line	Line	Line

Bits	Name	Description
27	CFRZ	Cache freeze. Allows the user to freeze the contents of the cache. When CFRZ is asserted line fetches can be initiated and loaded into the line-fill buffer, but a valid cache entry can not be overwritten. If a given cache location is invalid, the contents of the line-fill buffer can be written into the memory array while CFRZ is asserted. 0 Normal operation 1 Freeze valid cache lines
26–25	—	Reserved, should be cleared.
24	CINVA	Cache invalidate all. Writing a 1 to this bit initiates entire cache invalidation. Note the caches are not cleared on power-up or normal reset. 0 No invalidation is performed. 1 Initiate invalidation of the entire cache. The cache controller sequentially clears V in all sets. Subsequent accesses stall until invalidation finishes, at which point, CINVA is automatically cleared. This operation takes 64 clock cycles.
23–11	—	Reserved, should be cleared.
10	CEIB	Default noncacheable fill buffer. Determines if the fill buffer can store noncacheable accesses 0 Fill buffer not used to store noncacheable instruction accesses (16 or 32 bits). 1 Fill buffer used to store noncacheable accesses. The fill buffer is used only for normal (TT = 0) instruction reads of a noncacheable region. Instructions are loaded into the fill buffer by a burst access (same as a line fill). They stay in the buffer until they are displaced, so subsequent accesses may not appear on the external bus. Note that this feature can cause a coherency problem for self-modifying code. If CEIB = 1 and a cache-inhibited access uses the fill buffer, instructions remain valid in the fill buffer until a cache-invalidate-all instruction, another cache-inhibited burst, or a miss that initiates a fill.
9	DCM	Default cache mode. See Section 4.3.2.3, "Caching Modes." 0 Default cacheable 1 Default noncacheable
8	DBWE	Default buffered write enable. Defines the default value for enabling buffered writes. Generally, enabled buffered writes provide higher system performance but recovery from access errors can be more difficult. For the ColdFire CPU, reporting access errors on operand writes is always imprecise and enabling buffered writes simply further decouples the write instruction from the signaling of the fault. 0 Termination of an operand write cycle on the processor's local bus is delayed until the external bus cycle completes. 1 A local bus write cycle is terminated immediately and the operation buffered in the bus controller. Operand write cycles are effectively decoupled between the processor's local bus and the external bus.
7–6	—	Reserved, should be cleared.
5	DWP	Default write protect. 0 Read and write accesses permitted 1 Write accesses not permitted
4–2	—	Reserved, should be cleared.

Cache Programming Model

	31	24	23	16	15	14	13	12	7	6	5	4	3	2	1	0
Field	BA		BAM		EN	SM		—		CM	BWE	—	WP	—		
Reset	0000_0000_0000_0000															
R/W	Write (R/W by debug module)															
Rc	ACR0: 0x004; ACR1: 0x005															

Figure 4-5. Access Control Register Format (ACRn)

Bits	Name	Description
31–24	BA	Base address. Compared with A[31:24]. Eligible addresses that match are assigned the access control attributes of this register.
23–16	BAM	Base address mask. Setting a BAM bit masks the corresponding BA bit. Setting low-order BAM bits can define contiguous regions exceeding 16 Mbytes. BAM can define multiple noncontiguous regions.
15	EN	Enable. Enables or disables the other ACRn bits. 0 Access control attributes disabled 1 Access control attributes enabled

Bits	Name	Description
14–13	SM	Supervisor mode. Specifies whether only user or supervisor accesses are allowed in this address range or if the type of access is a don't care. 00 Match addresses only in user mode 01 Match addresses only in supervisor mode 1x Execute cache matching on all accesses
12–7	—	Reserved; should be cleared.
6	CM	Cache mode. Defines whether the memory access is cacheable or noncacheable. 0 Caching enabled 1 Caching disabled
5	BWE	Buffered write enable. Generally, the enabling of buffered writes provides higher system performance but recovery from access errors may be more difficult. For the ColdFire CPU, reporting access errors on operand writes is always imprecise; enabling buffered writes further decouples the write instruction from the signaling of the fault. 0 Termination of an operand write cycle on the processor's local bus is delayed until the external bus cycle is completed. 1 A write cycle on the local bus is terminated immediately and the operation is then buffered in the bus controller. In this mode, operand write cycles are effectively decoupled between the processor's local bus and the external bus.
4–3	—	Reserved, should be cleared.
2	WP	Write protect. Selects the write privilege of the memory region. 0 Read and write accesses permitted 1 Write accesses not permitted
1–0	—	Reserved, should be cleared.

SIM

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x000	Module base address register (MBAR), after initialization [p. 6-4]			
0x004	System configuration register (SCR) [p. 6-5]		System protection register (SPR) [p. 6-6]	
0x008	Power management register (PMR) [p. 6-7]			
0x00C	Reserved		Active low power register (ALPR) [p. 6-10]	
0x010	Device identification register (DIR) [p. 6-11]			
0x014–0x01C	Reserved			
Interrupt Controller Registers				
0x020	Interrupt control register 1 (ICR1) [p. 7-4]			
0x024	Interrupt control register 2 (ICR2) [p. 7-5]			
0x028	Interrupt control register 3 (ICR3) [p. 7-5]			
0x02C	Interrupt control register 4 (ICR4) [p. 7-6]			
0x030	Interrupt source register (ISR) [p. 7-6]			
0x034	Programmable interrupt transition register (PITR) [p. 7-7]			
0x038	Programmable interrupt wakeup register (PIWR) [p. 7-7]			
0x03C	Reserved			Programmable interrupt vector register (PIVR) [p. 7-8]
Software Watchdog Registers				
0x280	Watchdog reset reference register (WRRR) [p. 6-13]		Reserved	
0x284	Watchdog interrupt reference register (WIRR) [p. 6-13]		Reserved	
0x288	Watchdog counter register (WCR) [p. 6-14]		Reserved	
0x28C	Watchdog event register (WER) [p. 6-14]		Reserved	

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System Integration Module

- **The System Integration Module provides overall control and arbitration of the bus and serves as the interface between the ColdFire core and the internal peripheral devices**
- **It provides the following features:**
  - **Module base address register (MBAR)**
  - **Interrupt Controller**
  - **Chip Select module and SDRAM controller interface**
  - **System protection (watchdog timer)**
  - **Pin Assignment Register (PAR)**
  - **Power Management**
  - **Bus Arbitration**

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Chip Select Module

- **The ColdFire provides**
  - **8 dedicated chip selects**
  - **Address masking for memories ranging from 4K to 2 GB**
  - **Programmable wait states and port sizes**
  - **Programmable address setup and hold times**
  - **SDRAM controller interface with CS7#**
  - **Global chip select functionality**
  - **CS0# used to access external boot ROM, in conjunction with BUSW[1:0]**

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Chip Select Module

Offset	Name	Chip Select Register	Reset
+ 0x040	CSBR0	CS base register 0	0x0000_0x01[1]
+ 0x044	CSOR0	CS option register 0	0xFFFF_F078
+ 0x048	CSBR1	CS base register 1	0x0000_1300
+ 0x04C	CSOR1	CS option register 1	0xFFFF_F078
+ 0x050	CSBR2	CS base register 2	0x0000_2300
+ 0x054	CSOR2	CS option register 2	0xFFFF_F078
+ 0x058	CSBR3	CS base register 3	0x0000_3300
+ 0x05C	CSOR3	CS option register 3	0xFFFF_F078
+ 0x060	CSBR4	CS base register 4	0x0000_4300
+ 0x064	CSOR4	CS option register 4	0xFFFF_F078
+ 0x068	CSBR5	CS base register 5	0x0000_5300
+ 0x06C	CSOR5	CS option register 5	0xFFFF_F078
+ 0x070	CSBR6	CS base register 6	0x0000_6300
+ 0x074	CSOR6	CS option register 6	0xFFFF_F078
+ 0x078	CSBR7	CS base register 7	0x0000_7700
+ 0x07C	CSOR7	CS option register 7	0xFFFF_F078

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CS Base Address Register

31 12	11	10	9	8	7	6	5	4 2	1	0
BA	EBI		BW		SUPER	TT		TM	CTM	ENABLE
Reset: CSBR0: 0x0000_0x01[1]; CSBR1: 0x0000_1300; CSBR2: 0x0000_2300; CSBR3: 0x0000_3300; CSBR4: 0x0000_4300; CSBR5: 0x0000_5300; CSBR6: 0x0000_6300; CSBR7: 0x0000_7700										

Bits	Name	Description
31–12	BA	Base address. The starting address of the memory space covered by the chip select. BA is compared with bits 31–12 of the access to determine whether the current bus cycle is intended for this chip select. Any combination of BA bits can be masked in the associated CSOR.
11–10	EBI	External bus interface modes. These modes are used to multiplex outputs and determine timing of the appropriate bus interface module onto the device pins. 00 16–32-bit SRAM/ROM. For 16–32-bit wide memory devices with byte strobe inputs. CSBR0[EBI] = 00 at reset. Affects all chip selects. 01 SDRAM. One physical bank of SDRAM consisting of 16–256 Mbit devices. CSOR7[WS] must be set to 0x1F. Affects only CS7/SDCS. 10 Reserved 11 Use SRAM/ROM timing for 8-bit devices without byte strobe inputs.
9–8	BW	Bus width. Determines data bus size of the memory-mapped resource for all chip selects except CS0. It is assumed that boot code for the processor is accessed through the global chip select, CS0, so the initial bus width for this chip select must be configured at reset. GSPI_CS0/BUSW0 and GSPI_CLK/BUSW1 are used to program the bus width for CS0 at reset. 00 Longword (32 bits) 01 Byte (8 bits) 10 Word (16 bits) 11 Cache line (32 bits)
7	SUPER	Supervisor mode. 0 Bus cycle may be in user or supervisor mode (neglecting conditions imposed by setting CTM). 1 The chip select asserts a match only if the transfer modifier indicates a supervisor mode access. A user access matching BA causes an access error. SUPER, CTM, TT, and TM are used to restrict bus access. For example, if TT and TM indicate a user data access and SUPER and CTM are both set, no accesses can occur.
6–5	TT	Transfer type. TT and TM may be used to further qualify the address match. If CTM is set, TT and TM must match the access types for the chip select to assert. See the description of TM.

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CS Base Address Register

Bits	Name	Description
4–2	TM	Transfer modifier. Operates with TT to determine the access type. TT TM Function 0x 000 Reserved 0x 001 User data access 0x 010 User instruction access 0x 011–100 Reserved 0x 101 Supervisor data access 0x 110 Supervisor instruction access 0x 111 Reserved 10 000–100 Reserved 10 101 Emulator mode data access 10 110 Emulator mode instruction access 10 111 Reserved 11 000 CPU space access 11 001 Interrupt acknowledge level 1 11 010 Interrupt acknowledge level 2 11 011 Interrupt acknowledge level 3 11 100 Interrupt acknowledge level 4 11 101 Interrupt acknowledge level 5 11 110 Interrupt acknowledge level 6 11 111 Interrupt acknowledge level 7
1	CTM	Compare TM. Enables comparison between the access type and the TM and TT bits. 0 TT and TM register bits do not affect address match. 1 TT and TM register bits must match the access type for an address match to occur.
0	ENABLE	Enable. Disables/enables the chip select. When disabled, the chip select is never asserted, regardless of the address on the internal bus. ENABLE is 0 at reset, except CS0 which is 1. 0 Chip select is disabled, no matches can occur and chip select output cannot assert. 1 Chip select is enabled, bus cycles are compared against register contents.

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CS Option Register

	31 12	11	10	9	8	7	6 2	1	0
Field	BAM	ASET	WRAH	RDAH	EXTBURST	—	WS	RW	MRW
Reset	0xFFFF_F078								
R/W	R/W								
Addr	0x044 (CSOR0); 0x04C (CSOR1); 0x054 (CSOR2); 0x05C (CSOR3); 0x064 (CSOR4); 0x06C (CSOR5); 0x074 (CSOR6); 0x07C (CSOR7)								

Name	Name	Description
31–12	BAM	Address mask. Masks equivalent CSOR[BA] bits. The BAM setting chooses which BA bits to compare with the corresponding address bit to determine a match. 0 Mask address bit 1 Compare address bit
11	ASET	Address setup enable. Controls assertion of chip select with respect to assertion of a valid address that hits in the chip select address space. 0 Assert chip select on the rising edge of CLK that address is asserted. 1 Delay assertion of chip select for one CLK cycle after address is asserted. During write transfers, both chip select and R/$\overline{W}$ are delayed by 1 clock cycle. R/$\overline{W}$ asserts 1 clock cycle after assertion of the chip select.
10	WRAH	Controls the address, data, and attribute hold time after the termination, internal or external with $\overline{TA}$, of a write cycle that hits in the chip select address space. 0 Do not hold address, data, and attribute signals an extra cycle after chip select and R/$\overline{W}$ negate on writes. 1 Hold address, data, and attribute signals an extra cycle after $\overline{CSx}$ and R/$\overline{W}$ negate on writes.

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CS Option Register

Name	Name	Description
9	RDAH	Controls the address and attribute hold time after the termination, internal or external with $\overline{TA}$, of a read cycle that hits in the chip select address space. 0 Do not hold address and attribute signals an extra cycle after chip select negates on reads. 1 Hold address and attribute signals an extra cycle after chip select negate on reads.
8	EXTBURST	Enable extended burst. Valid only for $\overline{CS7}$. Reserved bit for $\overline{CS0}$:5]. EXTBURST should be 1 when external SDRAM is configured for a data bus narrower than the width programmed for the MCF5272. EBI must be set for SDRAM and the BW must be set to the data bus width of the external SDRAM array. Example: If the MCF5272 external physical data bus width is 32 or 16 bits but the external SDRAM is 16 bits wide, EXTBURST must be set and BW must be 10 (word) for $\overline{SDCS}$. 0 Extended bursts are not enabled. 1 Extended bursts are enabled.
7	—	Reserved, should be cleared.
6–2	WS	Wait state generator. Specifies the number of wait states (in system clocks) needed before the SIM generates an internal transfer acknowledge signal to terminate the access. 0x00 No wait states 0x01 1 wait state 0x1E 30 wait states 0x1F External access For example, WS = 0x0A introduces a 10-clock wait before the bus cycle terminates; 0x1F indicates a source external to the chip select module terminates the access. For SRAM and ROM accesses EBI codes 00 or 11 and WS = 0x1F, $\overline{TA}$ must be driven from an external source to terminate the bus cycle, otherwise the on-chip bus timeout monitor issues a bus error exception. For SRAM and ROM accesses with EBI = 00 or 11 and WS = 0x00–0x1E, the chip select module terminates the bus cycle after the programmed number of system clocks. For SDRAM accesses with $\overline{SDCS}$, EBI = 01, and WS = 0x1F, bus cycles are terminated under control of the SDRAM controller. The CSOR0[WS] reset default is 0x1E. The default for all other CSORs is 0x00. Caution: Never drive $\overline{TA}$ as an input to terminate SDRAM peripheral accesses.
1	RW	RW and MRW determine whether the selected memory region is read only or write only. 0 Read only 1 Write only
0	MRW	MRW must be set for value of RW be taken into consideration. 0 Memory covered by chip select is read/write. The memory covered by the chip select is neither read nor write protected. 1 RW determines whether memory covered by chip select is read only or write only. A conflict causes either a read or write protect violation.

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End of Lecture 1

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UART Module

- The 5272 contains two independent UARTs
- Each UART can be clocked by the CPU, or by an external source
- They each provide extensive interrupt control and baud rate selections, as well as full-duplex receive/transmitter functionality

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UART

- Features of the UART are:
  - 24 byte FIFO receiver with FIFO timeout
  - 24 byte FIFO transmitter
  - Independently programmable receiver and transmitter clock sources
  - Programmable data format, from 5-8 data bits, with various parity features and different numbers of stop bits
  - Each channel can be programmed for automatic echo, local loop-back, or remote loop-back mode
  - Automatic wake-up mode for multi-drop applications
- UART registers are only accessible as bytes

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UART Programming Model

MBAR Offset						
UART0	UART1	[31:24]	[23:16]	[15:8]	[7:0]	
0x11C	0x15C	(Read) Do not access.[1]			—	
		UART divider lower registers—(UDLx) [p. 16-14]			—	
0x120	0x160	(Read) UART autobaud register MSB—(UABAUn) [p. 16-15]			—	
		(Write) Do not access.[1]			—	
0x124	0x164	(Read) UART autobaud register LSB—(UABLx) [p. 16-15]			—	
		(Write) Do not access[2]			—	
0x128	0x168	UART Transmitter FIFO registers—(UTFx) [p. 16-5]			—	
0x12C	0x16C	UART Receiver FIFO registers—(URFx) [p. 16-5]			—	
0x130	0x170	UART Fractional Precision Divider Control registers (UFPDn) [p. 16-17]			—	
0x134	0x174	(Read) UART input port registers—(UIPn) [p. 16-18]			—	
		(Write) Do not access.[1]			—	
0x138	0x178	(Read) Do not access.[1]			—	
		(Write) UART output port bit set command registers—(UOP1n[3]) [p. 16-19]			—	
0x13C	0x17C	(Read) Do not access.[1]			—	
		(Write) UART output port bit reset command registers—(UOP0n[3]) [p. 16-19]			—	

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UART Mode Register 1

- **The UART Mode Register 1 (UMR1n) sets the configuration of the UART register such as parity mode and parity type**
- **It can be read or written when the mode register points to it**
- **After UMR1n has been read or written, the pointer then points to UMR2n**

	7	6	5	4	3	2	1	0
Field	RxRTS	RxIRQ/FFULL	ERR	PM		PT	B/C	
Reset	0000_0000							
R/W	R/W							
Address	MBAR + 0x100 (UART0), 0x140 (UART1). After UMR1n is read or written, the pointer points to UMR2n.							

Figure 16-2. UART Mode Registers 1 (UMR1*n*)

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UART Mode Register 2

- **The UMR2n further configures the UART by setting configuration such as the channel mode (normal, echo, or loop-back), stop bit length control**
- **It can be read or written when the mode register points to it, which is the case after a read/write of UMR1n**

	7	6	5	4	3	0
Field	CM		TxRTS	TxCTS	SB	
Reset	0000_0000					
R/W	R/W					
Address	MBAR + 0x100, 0x140. After UMR1n is read or written, the pointer points to UMR2n.					

Figure 16-3. UART Mode Register 2 (UMR2*n*)

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UART Command Register

- **The UART Command Registers UCRn supply commands to the UART module**
- **Only multiple commands that do not conflict can be specified at one time**
- **For example, RESET UART and ENABLE UART cannot be specified at the same time**

	7	6	4	3	2	1	0
Field	ENAB	MISC		TC		RC	
Reset	0000_0000						
R/W	Write only						
Address	MBAR + 0x108, 0x148						

Figure 16-6. UART Command Registers (UCR*n*)

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UCR Fields

Bits	Value	Command	Description
7	ENAB	—	Enable autobaud 0 Autobaud disabled. 1 Autobaud enabled. The transmission rate is calculated from the first received character. If the rate must be recalculated, ENAB must first be cleared and reset. UISRn[ABC] indicates a transmission rate has been calculated and loaded into the UART divider registers. UDUn and UDULn must be initialized to 0x00 before enabling autobaud.
6–4		**MISC Field** (This field selects a single command.)	
	000	NO COMMAND	—
	001	RESET MODE REGISTER POINTER	Causes the mode register pointer to point to UMR1n.
	010	RESET RECEIVER	Immediately disables the receiver, clears USRn[FFULL,RxRDY], and reinitializes the receiver FIFO pointer. No other registers are altered. Because it places the receiver in a known state, use this command instead of RECEIVER DISABLE when reconfiguring the receiver.
	011	RESET TRANSMITTER	Disables the transmitter and clears USRn[TxEMP,TxRDY]. No other registers are altered. Because it places the transmitter in a known state, use this command instead of TRANSMITTER DISABLE when reconfiguring the transmitter.
	100	RESET ERROR STATUS	Clears USRn[RB,FE,PE,OE]. Also used in block mode to clear all error bits after a data block is received.
	101	RESET BREAK-CHANGE INTERRUPT	Clears the delta break bit, UISRn[DB].
	110	START BREAK	Forces TxD low. If the transmitter is empty, the break may be delayed up to one bit time. If the transmitter is active, the break starts when character transmission completes. The break is delayed until any character in the transmitter shift register is sent. Any character in the transmitter holding register is sent after the break. The transmitter must be enabled for the command to be accepted. This command ignores the state of CTS.
	111	STOP BREAK	Causes TxD to go high (mark) within two bit times. Any characters in the transmitter buffer are sent.
3–2		**TC Field** (This field selects a single command)	
	00	NO ACTION TAKEN	Causes the transmitter to stay in its current mode: if the transmitter is enabled, it remains enabled; if the transmitter is disabled, it remains disabled.
	01	TRANSMITTER ENABLE	Enables operation of the channel's transmitter. USRn[TxEMP,TxRDY] are set. If the transmitter is already enabled, this command has no effect.
	10	TRANSMITTER DISABLE	Terminates transmitter operation and clears USRn[TxEMP,TxRDY]. If a character is being sent when the transmitter is disabled, transmission completes before the transmitter becomes inactive. If the transmitter is already disabled, the command has no effect.
	11	—	Reserved, do not use.

UCR Fields

Bits	Value	Command	Description
1–0		**RC** (This field selects a single command)	
	00	NO ACTION TAKEN	Causes the receiver to stay in its current mode. If the receiver is enabled, it remains enabled; if disabled, it remains disabled.
	01	RECEIVER ENABLE	If the UART module is not in multidrop mode (UMR1n[PM] ≠ 11), RECEIVER ENABLE enables the channel's receiver and forces it into search-for-start-bit state. If the receiver is already enabled, this command has no effect.
	10	RECEIVER DISABLE	Disables the receiver immediately. Any character being received is lost. The command does not affect receiver status bits or other control registers. If the UART module is programmed for local loop-back or multidrop mode, the receiver operates even though this command is selected. If the receiver is already disabled, the command has no effect.
	11	—	Reserved, do not use.

UART Receive Buffer

- **The Receive buffer contains one serial shifter and a 24 byte FIFO**
- **The CPU reads from the top of the stack while the RxD shifts and updates from the bottom**
- **RB contains the character in the receiver**

	7 … 0
Field	RB
Reset	0000_0000
R/W	Read only
Address	MBAR + 0x10C,0x14C

Figure 16-7. UART Receiver Buffer (URBn)

UART Transmitter Buffer

- **The Transmitter also consists of a 24 byte buffer and a transmit shift register**
- **The transmitter automatically inhibits writing of any more characters while the FIFO is full**

7		0
Field	TB	
Reset	0000_0000	
R/W	Write only	
Address	MBAR + 0x10C,0x14C	

Figure 16-8. UART Transmitter Buffers (UTBn)

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UART – Multidrop

- **The MCF5272 UART has an advanced feature enabling it to operate in a wake-up mode for multi-drop or multi-processor applications**
- **In this mode a master can transmit an address character followed by a block of data characters targeted for one of up to 256 slaves**
- **The slaves have their receivers disabled, but they still continue to monitor the master's data stream**

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UART – Multidrop

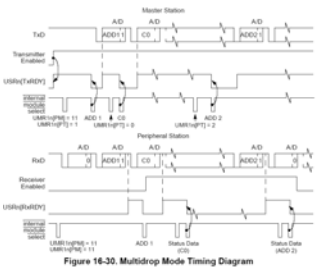

Figure 16-30. Multidrop Mode Timing Diagram

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GPIO

- **The MCF5272 provides up to 48 General Purpose IO ports**
- **The GPIO ports are multiplexed with other module signals and must be selected appropriately**
- **To avoid indeterminate read values and reduce power consumption, internal pull-up resistors are active immediately after a reset**

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GPIO registers

MBAR Offset	[31:24]	[23:16]	[15:8]	[7:0]
0x0080	Port A Control Register (PACNT)			
0x0084	Port A Data Direction Register (PADDR)		Reserved	
0x0086	Reserved		Port A Data Register (PADAT)	
0x0088	Port B Control Register (PBCNT)			
0x008C	Port B Data Direction Register (PBDDR)		Reserved	
0x008E	Reserved		Port B Data Register (PBDAT)	
0x0094	Port C Data Direction Register (PCDDR)		Reserved	
0x0096	Reserved		Port C Data Register (PCDAT)	
0x0098	Port D Control Register (PDCNT)			

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Port A Control Register

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	PACNT15		PACNT14		PACNT13		PACNT12		PACNT11		PACNT10		PACNT9		PACNT8	
Reset	0000_0000_0000_0000															
R/W	Read/Write															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	PACNT7		PACNT6		PACNT5		PACNT4		PACNT3		PACNT2		PACNT1		PACNT0	
Reset	0000_0000_0000_0000															
R/W	Read/Write															
Addr	MBAR + 0x0080															

Figure 17-1. Port A Control Register (PACNT)

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PACNT

Bits	Name	Description
31–30	PACNT15	Configure pin M3. If this pin is programmed to function as $\overline{INT7}$, it is not available as a GPIO. 00 PA15 01 DGNT1 1x Reserved
29–28	PACNT14	Configure pin M2 00 PA14 01 DREQ1 1x Reserved
27–26	PACNT13	Configure pin L3 00 PA13 01 DFSC3 1x Reserved
25–24	PACNT12	Configure pin L2 00 PA12 01 DFSC2 1x Reserved
23–22	PACNT11	Configure pin L1 00 PA11 01 Reserved 10 QSPI_CS1 11 Reserved
21–20	PACNT10	Configure pin K5 00 PA10 01 DREQ0 1x Reserved
19–18	PACNT9	Configure pin J3 00 PA9 01 DGNT0 1x Reserved

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PADDR

	15	0
Field	PADDR	
Reset	0000_0000_0000_0000	
R/W	Read/Write	
Addr	MBAR + 0x0084	

Figure 17-4. Port A Data Direction Register (PADDR)

Table 17-9. PADDR Field Descriptions

Bits	Name	Description
15–0	PADDR	Data direction bits. Each data direction bit selects the direction of the signal as follows: 0 Signal is defined as an input. 1 Signal is defined as an output.

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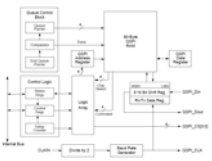
Queued SPI

- **Programmable queue to support up to 16 transfers without user intervention**
- **Supports transfer sizes of 8 to 16 bits in 1-bit increments**
- **Four peripheral chipselect lines to control up to 15 devices**
- **Baud rates from 129.4 Kbps to 33 Mbps at 66 MHz**
- **Programmable delays before and after transfers**



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QSPI

- The QSPI uses a dedicated 80 byte SRAM to provide for:
  - 16 command control bytes
  - 16 data write bytes
  - 16 data read bytes
- Each byte corresponds to one queue entry from 0x00 to 0x0F

Relative Address	Register	Function
0x00	QTR0	Transmit RAM
0x01	QTR1	16 bits wide
...	...	
0x0F	QTR15	
0x10	QRR0	Receive RAM
0x11	QRR1	16 bits wide
...	...	
0x1F	QRR15	
0x20	QCR0	Command RAM
0x21	QCR1	8 bits wide
...	...	
0x2F	QCR15	

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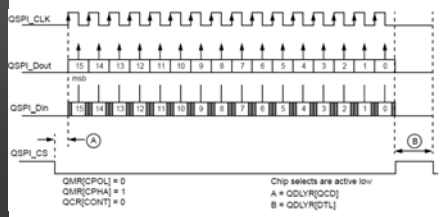
QSPI

- Clocking and Data Transfer Example



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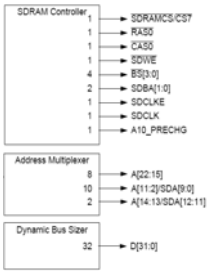
SDRAM Controller

- The MCF5272 SDRAM controller provides a glueless interface to a variety of SDRAM devices
- Data bus width sizes of 16 or 32
- 16- to 256-Mbit device support



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DMA Controller

- **The 5272 provides a one-channel DMA controller which supports memory-to-memory transfers that can be used for block-data moves**
- **The DMA Mode Register controls various DMA operations, in particular that of addressing modes**

	31	30	29		20	19	18	17	16
Field	RESET	EN	—			RQM	—		
Reset	0000_0000_0000_0000								
R/W	R/W								

	15	14	13	12	10	9	8	7	6	5	4	2	1	0
Field	—	DSTM	DSTT		DSTS		—	—	SRCM	SRCT				SRCS
Reset	0	01	1_00		01		0	0	1	1_01				01
R/W	R/W													
Addr	MBAR + 0x00E0													

Figure 10-1. DMA Mode Register (DMR)

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DMR

Bits	Name	Description
31	RESET	Reset. Writing a 1 to this location causes the DMA controller to reset to a condition where no transfers are taking place. EN is cleared, preventing new transfers.
30	EN	Enable. Controls whether the DMA channel is enabled to perform transfers. 0 DMA transfers are disabled 1 DMA transfers are enabled. The DMA controller can respond to requests from the peripheral or generates internal requests in dual address mode, so long as the conditions described under Table 10-3. Interrupt Register Sections 10.3.2, "DMA Interrupt Register (DIR)") do not prevent transfers from going on.
29–20	—	Reserved, should be cleared.
19–18	RQM	Request mode. Determines the request mode of the channel. This must be 11. 00–10 Reserved, do not use. 11 Dual address request mode. Both the DMA source and DMA destination are memory addresses. The MCF5272 supports only dual-address request mode.
17–15	—	Reserved, should be cleared.
14–13	DSTM	Destination addressing mode for the channel. 00 Static address mode 01 Incrment address mode 1x Reserved, do not use.
12–10	DSTT	Destination addressing type. Used internal to the MCF5272 to qualify the address bits. This value should be compatible with the CSCRn(TM) value used for external RAM or peripheral device access. 000 Reserved 001 User data access 010 User code access 011–100 Reserved 101 Supervisor data access 110 Supervisor code access 111 Reserved
9–8	DSTS	Destination data transfer type. The DMA controller buffers data from the source address data fetches until there are enough bytes to perform a destination data write of the size programmed in these bits. Thus it is possible to configure source accesses to be byte type and destination addresses to be line burst type. In this case 16 individual byte reads are performed followed by an indivisible burst write of four longwords. Longword or line bursts are the most efficient data transfers.
7	—	Reserved, should be cleared.
6	—	Reserved, should be cleared.
5	SRCM	Source addressing mode of the channel. 0 Static address mode 1 Incrment address mode

DSTS	Data Transfer Type	Address Incremented by
00	Longword	4
01	Byte	1
10	Word	2
11	16-byte line burst	16. Valid only for SDRAM.

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DMR

Bits	Name	Description
4–2	SRCT	Source addressing type. Used internal to the MCF5272 to qualify the address bits. The value should be compatible with the CSCRn(TM) value used for external RAM or peripheral device access. 000 Reserved 001 User data access 010 User code access 011 Reserved 100 Reserved 101 Supervisor data access 110 Supervisor code access 111 Reserved
1–0	SRCS	Source data transfer type. Determines the amount of data the DMA controller fetches and buffers data from the source address. When there are enough bytes to perform a destination data write of the size programmed in DSTS, the data is written to the the destination address. Thus source accesses can be longword type and destination addresses can be line burst type. In this case, 4 longword reads are performed followed by an indivisible burst write of 4 longwords. The most efficient data transfer method is to use longword or line burst transfer types.

SRCS	Data Transfer Type	Address Incremented by
00	Longword	4
01	Byte	1
10	Word	2
11	16-byte line burst	16. Valid only for SDRAM.

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DMA Address Registers

- The DMA Source Address Register (DSAR) provides a 32-bit address which the DMA controller drives onto the internal bus for all the channel's read accesses
- In the same fashion, the DMA Destination Address Register (DDAR) provides the address which the DMA controller provides to the bus for all write operations
- The DMA Byte Count Register (DBCR) provides the number of bytes which need to be transferred

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Ethernet Module

- Full compliance with IEEE 802.3 standard
- Supports three different physical interfaces
  - 100 Mbps Media Independent Interface (MII)
  - 10 Mbps MII
  - 10 Mbps seven-wire interface
- 448 byte on-chip transmit and receive FIFO, which works in conjunction with the DMA engine

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Fast Ethernet Controller

- The Fast Ethernet Controller is designed to work with little host intervention
- As soon as the driver enables the FEC transmitter, the FEC fetches the first FEC transmit buffer descriptor (TxBD), and if there is a frame ready to be transferred, the DMA transmit of the data buffer starts immediately

NOTE: Short Tx frames are padded automatically by the MCF5272

Figure 11-3. Ethernet Frame Format

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FEC

- When the transmit FIFO contains 512 bits of data, the FEC asserts the E_TxEN and starts transmitting the preamble sequence, the start-of-frame delimiter, and then the frame data
- If the line is busy, the controller defers transmission (carrier sense is active)
- If the carrier sense goes inactive, the controller waits to verify that it stays inactive for 60 bit times, and if so, the transmission begins after waiting an additional 36 bit times
- If a collision occurs, the FEC follows the specified back-off procedures and retransmits until the retry limit is reached
- The FEC stores the first 64 bytes of the transmit frame in internal RAM so it doesn't need to be retrieved

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Ethernet Programming Model

Offset	Name	Width	Description
0x840	ECR	32	Ethernet control register. [p. 11-12]
0x844	EIR	32	Interrupt event register. [p. 11-13]
0x848	EIMR	32	Interrupt mask register. [p. 11-14]
0x84C	IVSR	32	Interrupt vector status register. [p. 11-14]
0x850	RDAR	32	Receive descriptor active register. [p. 11-15]
0x854	TDAR	32	Transmit descriptor active register. [p. 11-16]
0x880	MMFR	32	MII management frame register. [p. 11-17]
0x884	MSCR	32	MII speed control register. [p. 11-18]
0x8CC	FRBR	32	FIFO receive bound register. [p. 11-20]
0x8D0	FRSR	32	FIFO receive start register. [p. 11-20]
0x8EC	TFSR	32	FIFO transmit start register. [p. 11-22]
0x8E4	TFWR	32	Transmit FIFO watermark. [p. 11-21]
0x944	RCR	32	Receive control register. [p. 11-23]
0x948	MFLR	32	Maximum frame length register. [p. 11-24]
0x964	TCR	32	Transmit control register. [p. 11-25]
0xC00	MALR	32	Lower 32-bits of MAC address
0xC04	MAUR	32	Upper 16-bits of MAC address
0xC08	HTUR	32	Upper 32-bits of hash table. [p. 11-27]
0xC0C	HTLR	32	Lower 32-bits of hash table. [p. 11-27]
0xC10	ERDSR	32	Pointer to receive descriptor ring. [p. 11-28]
0xC14	ETDSR	32	Pointer to transmit descriptor ring. [p. 11-29]
0xC18	EMRBR	32	Maximum receive buffer size. [p. 11-29]
0xC40 - 0xDFF	EFIFO	32	FIFO RAM space

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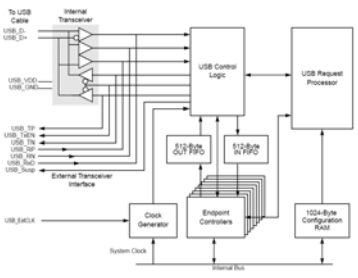
Universal Serial Bus



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USB

- USB uses four wires, two for data and two for power, and operates at a full data rate of 12Mbps
- The MCF5272 USB includes the following features
  - Full compliance with USB 1.1
  - Supports either internal or external USB transceiver
  - Programmable 512 byte receive and transmit FIFO buffers
  - USB device controller with protocol control and administration for up to eight endpoints, 16 interfaces, and 16 configurations
  - Independent interrupts for each endpoint
  - Remote wakeup

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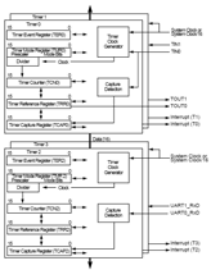
Timer Module

- The Timer module has four identical general-purpose 16-bit timers and a software watchdog timer
- Maximum period of 4 seconds at 66 MHz
- 15-ns resolution
- Programmable clock sources
- Free run and restart modes



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Timer

- A timer can be configured to count until a reference is reached, at which point it can either start a new time count immediately, or continue to run.
- Upon reaching a reference value, the timer can issue an interrupt
- Also, timers 0 and 2 are capable of outputting a signal on the timer outputs TOUT0 and TOUT1, which can be either an active-low pulse or a toggle of the current output
- Timers are also capable of latching counter values when the corresponding input capture edge detector detects a predefined transition, and this too can generate an interrupt

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Timer Mode Register

	15 … 8	7	6	5	4	3	2	1	0
Field	PRESCALER (PS)	CE		OM	ORI	FRR	CLK		RST
Reset	0000_0000_0000_0000								
R/W	Read/Write								
Addr	MBAR + 0x200 (TMR0); 0x220 (TMR1); 0x240 (TMR2); 0x260 (TMR3)								

Bits	Name	Description
15–8	PS	Prescaler. Programmed to divide the clock input by values from 1 to 256. The value 0000_0000 divides the clock by 1; the value 1111_1111 divides the clock by 256.
7–6	CE	Capture edge and enable interrupt 00 Disable capture and interrupt on capture event 01 Capture on rising edge only and generate interrupt on capture event 10 Capture on falling edge only and generate interrupt on capture event 11 Capture on any edge and generate interrupt on capture event
5	OM	Output mode (TMR0 and TMR1 only. Reserved in TMR2 and TMR3) 0 Active-low pulse for one system clock cycle (15 nS at 66 MHz) 1 Toggle output TOUTn is high at reset but is unavailable externally until the appropriate port control register is configured for this function. See Section 17.2, "Port Control Registers."
4	ORI	Output reference interrupt enable 0 Disable interrupt for reference reached (does not affect interrupt on capture function) 1 Enable interrupt upon reaching the reference value if ORI is 1 when the TER[REF] is set, an immediate interrupt occurs.
3	FRR	Free run/restart 0 Free run. Timer count continues to increment after the reference value is reached. 1 Restart. Timer count is reset immediately after the reference value is reached.
2–1	CLK	Input clock source for the timer 00 Stop count 01 Master system clock 10 Master system clock divided by 16. TIN0 and TIN1 are external to the MCF5272 and are not synchronized to the system clock, so successive timeout lengths may vary slightly. 11 Corresponding TIN pin. TIN0 or TIN1 (falling edge), unused in TMR2 and TMR3 The minimum high and low periods for TIN as the clock source is 1 system clock, which gives a maximum TIN frequency of clock/2.
0	RST	Reset timer. 0 A transition from 1 to 0 resets the timer. Other register values can be written. The counter/timer/prescaler are not clocked unless the timer is enabled. 1 Enable timer

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Timer Operation

	15 … 0
Field	REF (16-bit reference value)
Reset	1111_1111_1111_1111
R/W	Read/Write
Addr	MBAR + 0x204 (TRR0); 0x224 (TRR1); 0x244 (TRR2); 0x264 (TRR3)

Figure 15-3. Timer Reference Registers (TRR0–TRR3)

	15 … 0
Field	CAP (16-bit capture counter value)
Reset	0000_0000_0000_0000
R/W	Read Only
Addr	MBAR + 0x200 (TCAP0); 0x220 (TCAP1); 0x240 (TCAP2); 0x260 (TCAP3)

Figure 15-4. Timer Capture Registers (TCAP0–TCAP3)

	15 … 0
Field	COUNT (16-bit timer counter value)
Reset	0000_0000_0000_0000
R/W	Read/Write
Addr	MBAR + 0x20C (TCN0); 0x22C (TCN1); 0x24C (TCN2); 0x26C (TCN3)

Figure 15-5. Timer Counter (TCN0–TCN3)

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Timer Operation

	15 … 2	1	0
Field	—	REF	CAP
Reset	0000_0000_0000_0000		
R/W	Read/Write		
Addr	MBAR + 0x210 (TER0); 0x230 (TER1); 0x250 (TER2); 0x270 (TER3)		

Figure 15-6. Timer Event Registers (TER0–TER3)

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Mechanical Data

Figure 22-1. MCF5272 Pinout (196 MAPBGA)

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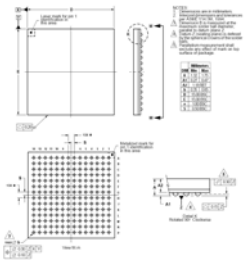
Mechanical Data



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Electrical Characteristics

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to + 4.0	V
Maximum operating voltage	V_{DD}	+3.6	V
Minimum operating voltage	V_{DD}	+3.0	V
Input voltage	V_{in}	–0.5 to +5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

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