Planarization of a CMOS die for an integrated metal MEMS

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ABSTRACT

This paper describes a planarization procedure to achieve a flat CMOS die surface for the integration of a MEMS metal mirror array. The CMOS die for our device is 4 mm x 4 mm and comes from a commercial foundry. The initial surface topography has 0.9 μm bumps from the aluminum interconnect patterns that are used for addressing the individual micro mirror array elements. To overcome the tendency for tilt error in the planarization of the small CMOS die, our approach is to sputter a thick layer of silicon nitride (2.2 μm) at low temperature and to surround the CMOS die with dummy pieces to define the polishing plane. The dummy pieces are first lapped down to the height of the CMOS die, and then all pieces are polished. This process reduces the 0.9 μm height of the bumps to less than 25 nm.

Keywords: Chemical mechanical planarization, MEMS mirror array, sputtering, polishing, MEMS integration

1. INTRODUCTION

Large arrays of micromachined piston-motion mirrors are required for laser communication and optical correlation applications. To control large numbers of pixels in a MEMS spatial light modulator array, it is necessary to address the pixels through direct integration, rather than off-chip addressing through many wire bond connections.[1] Such integration poses a system-level design challenge since the commercial foundry processes of the silicon MEMS are generally incompatible with prefabricated CMOS electronics.

A MEMS fabrication alternative based on metal micromachining has proven successful in the past for production of large micromirror arrays, notably for the Texas Instruments Digital Light Processor®.[2] Because all CMOS interconnects are formed with aluminum, subsequent processes should take place at temperatures below 450ºC to avoid rapid aluminum degradation.[3] For planarization of a CMOS die or wafer for metal MEMS, the polymer benzocyclobutene (BCB), which has been used for multichip module applications. It has a low hard cure temperature of 200-250 ºC. A multi layer structure of SiO_2/BCB/SiO_2 produced just 5% planarization error but left an edge bead that required subsequent removal.[4] Another BCB coating application successfully reduced the surface topography from 2.8 μm to about 60 nm.[5] Recently, chemical mechanical planarization (CMP) has become a key manufacturing technology for the IC industry, allowing higher density designs with an end-of-line process for metal interconnection.[6] It has been mostly applied to interlayer dielectric and metal damascene planarization. Also, CMP technology is used to make multi-level polysilicon MEMS structures. An integration scheme was developed that embeds the micromechanical devices in trenches (6-12 μm deep). This was followed by CMP of the MEMS wafer and conventional CMOS processing.[7] This approach configures the CMOS electronics and MEMS structures horizontally.

Our MEMS development project makes use of CMOS in die form. Planarization of small chips presents different challenges than planarization of wafers. This paper describes the process we adopted along with results.

2. LARGE-SCALE METAL MEMS

2.1 Large-scale metal MEMS description

A large array of electrostatically actuated, piston-motion MEMS mirror segments is under development at Boston University to be used as a spatial light modulator (μSLM) device for an adaptive optics application.[1] Figure 1 illustrates an example of mirror segments of the μSLM. The full array consists of 1024 mirror segments fabricated in aluminum over a 4 mm square aperture. Each pixel is capable of altering the phase of reflected light by up to one wavelength infrared light (λ=1.5 μm). An underlying CMOS driver provides 50 nm position resolution over 750 nm of stroke. Mirror elements must be optically flat and smooth and more than 90% reflective. The pixels are designed to have a step

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response time of 10 μs. This design achieves a mirror fill factor of 98%. Because the device is integrated directly with the underlying electronics, it is scalable to mega-pixel array sizes. Two significant challenges associated with manufacturing the μSLM are integration of the MEMS array with the CMOS electronic driver array, and production of optical-quality mirror elements using a metal-polymer micromachining process.

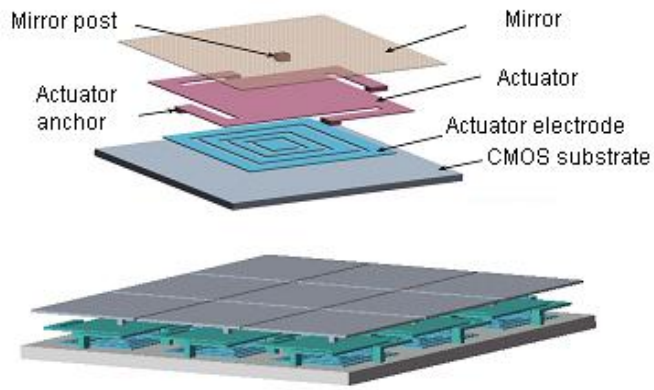


Figure 1. Metal MEMS configuration on the CMOS die

2.2 CMOS profile measurement

Figure 2(a) shows a corner of the CMOS die as received. It consists of interconnects for mirror actuation and bond pads. The 4 mm x 4 mm die has a 32 x 32 array of interconnects. Each actuator has connections for 8 electrodes as shown in Fig. 2(b). The foundry etched the passivation layer down to the aluminum layer in these 8 places to form vias.

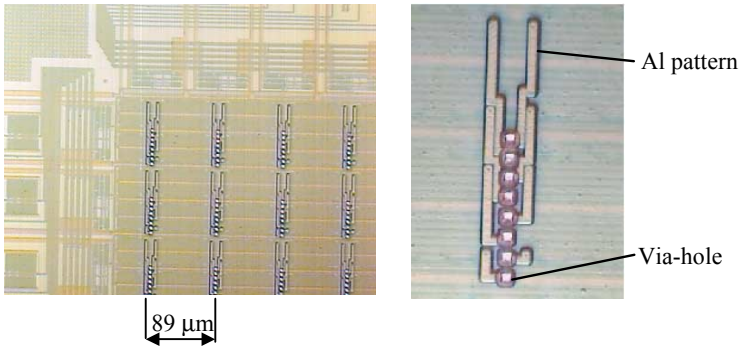
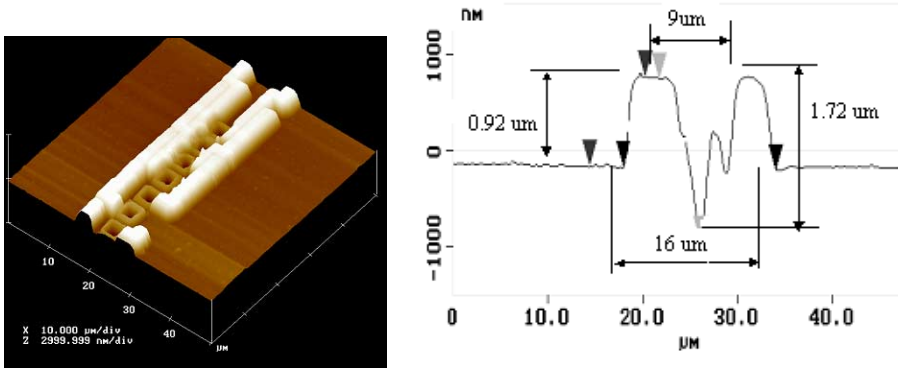


Figure 2. Micrograph of CMOS (a) interconnect arrangement and (b) multiple bit via-holes

The topography of the CMOS surface near the via-holes was investigated using atomic force microscope (AFM). Figure 3(a) shows a three-dimensional image. Conformal deposition of the passivation layer to cover the underlying aluminum pattern results in bumps 1.72 μm high relative to the aluminum layer at the bottom of the hole (see Fig. 3(b)). The bump height relative to the unetched outside surface (equivalent to the aluminum layer thickness) is 0.92 μm. The passivation structure (approximated above as 1.72 μm thick) of the CMOS die consists of a silicon dioxide layer on the bottom, which is about half of the total thickness, and a silicon nitride layer on top. The bumps of 0.92 μm height are to be removed through chemical mechanical planarization.



(a) (b)

Figure 3. AFM measurement of the bumps in the CMOS: (a) 3-D image; (b) Section profile

3. LOW TEMPERATURE DEPOSITION

3.1 Temperature characteristic of sputtering

The thickness of the passivation layer leaves little room for tilt error during the planarization process. Therefore, additional deposition of either silicon nitride or silicon dioxide was considered. Low temperature deposition is required to avoid damage to the metallic CMOS circuitry. Both silicon dioxide and silicon nitride have been deposited as interlayer dielectric materials at relatively low temperature using plasma enhanced chemical deposition (PECVD).[8] Silicon dioxide mostly functions as an electrical insulating layer while silicon nitride provides environmental protection from sodium ions. Our study pursued another deposition technique, RF sputtering. First, the temperature characteristic for the RF sputtering of two materials was measured. The RF sputtering machine was a Plasma-Therm 790®, and the sputtering target materials were of 99.9% purity.** Sputtering was done at a power setting of 351W, an argon flow rate of 75 sccm, and an initial vacuum pressure of 6.6×10^{-5} Pa. After pre-sputtering for a few minutes to get a stable plasma state, the sputtering temperature was recorded using a temperature gauge inside the vacuum chamber. Figure 4 shows how the temperature changes with time for the two materials.

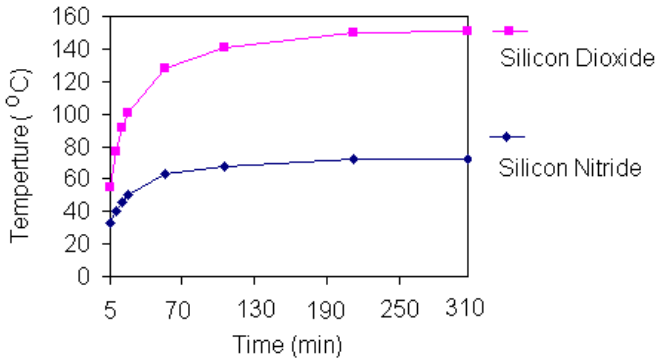


Figure 4. Temperature characteristic for RF sputtering of two passivation materials

The nominal room temperature was 21ºC, and two minutes of pre-sputtering increased the chamber temperature to 26ºC for silicon dioxide and 23ºC for silicon nitride. In about 60 minutes, temperatures reached about 90 percent of their final equilibrium values. The final silicon dioxide and silicon nitride temperatures are 156ºC and 75ºC, respectively. Repetition of the tests showed no more than a 10 percent variation in the results. These findings ensure that sputtering temperatures will remain well below the aluminum degradation temperature of 450ºC.

** Certain commercial equipment, instruments, or materials are identified in this paper to foster understanding. Such identification does not imply recommendation or endorsement by authors, nor does it imply that the materials or equipment identified are necessary the best available for the purpose

3.2 Sputter rate

The sputter rate of the two materials was measured while sputtering using the same power (351W) and flow rate (75 sccm) as above. Table 1 shows the total measured thickness of silicon dioxide after 242 minutes of sputtering. Each sample was scanned two times with a stylus profiler. The total variation in thickness values is 227 nm or 7% of the average thickness of 3243 nm. The standard deviation is 104 nm or 3.1% of the average thickness. Based on the mean thickness and total sputter time, the average sputter rate of the silicon dioxide was 13.4 nm/min.

Table 1. Sputter thickness of silicon dioxide after 242 minutes

Sample	1st scan (nm)	2nd scan (nm)	Mean (nm)
1	3197	3165	3181
2	3227	3215	3221
3	3287	3305	3296
4	3352	3392	3372
5	3267	3025	3146
Mean	3266	3220	3243

Table 2 shows the total measured thickness of silicon nitride after 75 minutes of sputtering. Thickness was measured three times for each sample. The variation in values is 70 nm or 9% of the 763 nm average thickness. The standard deviation is 18 nm or 2.4% of the average thickness. The average sputter rate of the silicon nitride was 10.2nm/min. The silicon dioxide sputtering rate is about 30% higher than for silicon nitride, but the uniformity in thickness values is similar.

Table 2. Sputter thickness of silicon nitride after 75 minutes

Sample	1st scan (nm)	2nd scan (nm)	3rd scan (nm)	Mean (nm)
1	753	740	765	753
2	778	763	725	755
3	773	760	733	755
4	778	740	775	764
5	763	750	758	757
6	773	775	788	779
7	793	770	775	780
Mean	773	757	760	763

Because much work has already been done to develop the oxide CMP, silicon dioxide would seem preferable as the deposition material. However, a thick layer of silicon dioxide would be needed to avoid polishing a mixed surface state of the sputtered silicon dioxide and the top passivation layer of silicon nitride. Different polishing rates for the two materials would lead to irregularities in the surface profile. Therefore, silicon nitride was chosen as the sputtering material that would subsequently be planarized. Additional sputtering rate tests were done with silicon nitride and are presented in Fig. 5. Initial chamber pressures for the six tests ranged between 1.3×10^{-5} Pa and 4.2×10^{-5} Pa. The other conditions were the same as in previous experiments. For the 28 minute and 280 minute tests, the sputter rates were 11.4 nm/min and 9.1 nm/min, respectively. The sputter rate tends to decrease with time but stabilizes after 170 minutes (1.56 μm thickness). The time for reaching steady-state matches well with the temperature characteristics in Fig. 4. An additional experiment of 450 minutes duration showed a sputter rate of 9.3 nm/min.

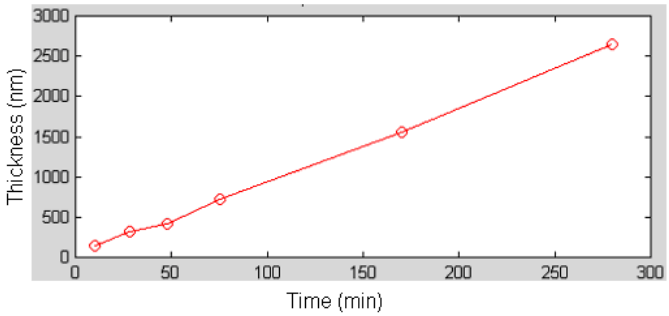


Figure 5. Sputter thickness of silicon nitride with time

4. CHEMICAL MECHANICAL PLANARIZATION

4.1 Configuration of lapping and polishing

Lapping and polishing were performed using Strasbaugh Polishmaster Spindles** with pneumatic platen pressure and automatic drip slurry. Figure 6 shows a schematic of the lapping/polishing setup. The 4 mm x 4 mm CMOS die is bonded using wax to a glass plate. Eight "dummy" 10 mm x 10 mm silicon pieces are bonded around the outer edge of the glass plate. These pieces were initially slightly thicker than the 300 µm thickness of the CMOS die. The lapping plate (with or without polishing pad on top) attaches to a rotating spindle. The glass plate (with attached pieces) reciprocates left and right and is free to rotate.

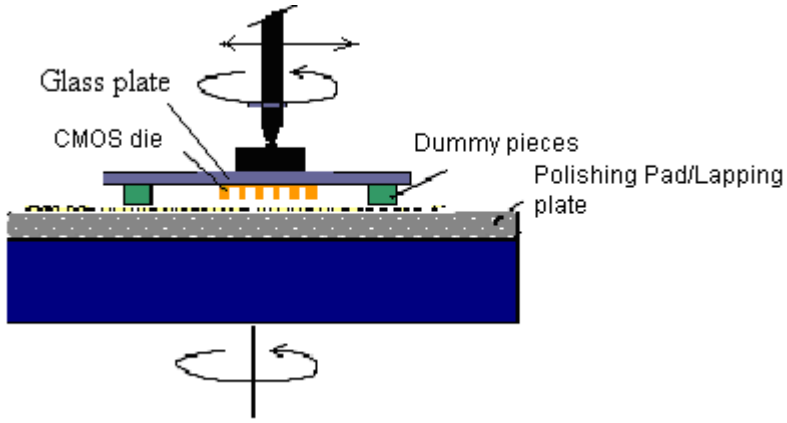
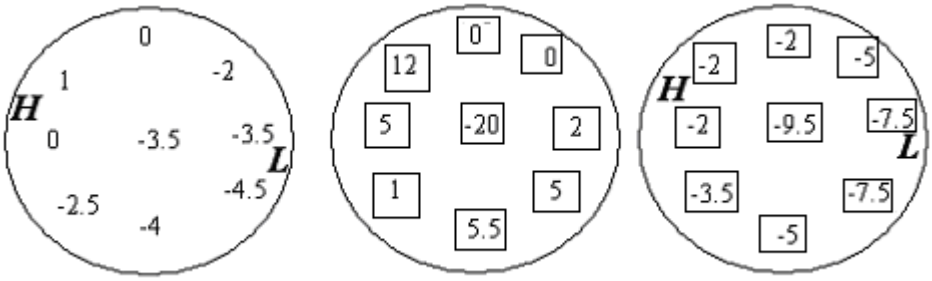


Figure 6. Lapping and polishing configuration

4.2 Lapping results

Lapping was used to even out the heights of the dummy pieces and to set the polishing plane. The lapping slurry was Al_2O_3 powder of 3 µm and 5 µm sizes, and the lapping plate was cast iron. To achieve CMOS planarization with minimal tilt error, the flatness of the glass plate is critical. The glass plate thickness was measured at nine locations (eight mounting points for dummy pieces and a center mounting point for the CMOS die) using a mechanical height gauge. A sample measurement result is shown in Fig. 7. The height distribution in Fig. 7(a) shows that the glass plate has a high and a low region with a difference of 4.5 µm between the two. After attaching a CMOS die and dummy pieces, the height of the pieces on the glass was measured with one result given in Fig. 7(b). Even though the silicon dummy pieces all have the same nominal thickness, variations in wax thickness cause the height difference to increase to 12 µm. After lapping for 20 minutes with 5 µm slurry followed by 10 minutes with 3 µm slurry, all pieces were measured again. Based on visual observation, the CMOS die was not touched by the lapping. The height distribution among the dummy pieces after lapping, as shown in Fig. 7(c), was consistent with that of the glass plate alone: the maximum height difference after lapping is 5.5 µm. Given that the diameter of the dummy piece circle is 80 mm, the height slope is about 0.07 µm/mm. This is the slope of the lapping plane relative to the bottom surface of the glass plate. However, the plane of the CMOS die could be different than the dummy piece plane. This would cause the subsequent polishing process to produce a tilt error in the CMOS chip surface.



(a) Glass plate (b) After attaching pieces (c) After lapping

Figure 7. Height measurements (in μm) of glass plate, CMOS chip and dummy pieces

4.3 Polishing results

Even when the lapping plane has not yet contacted the CMOS piece, a switch to polishing may produce contact. That can happen because the polishing pad is soft and deflects during polishing. A height gauge was used to measure the deflection of the glass plate (with pieces attached) as upper platen pressure was applied. Figure 8 shows the amount of deflection for 5 air pressure levels. The applied pressure also causes the lapping plate to deflect down slightly. This deflection is also shown in the figure and should be subtracted from the glass plate deflection to yield the pad deflection. At 30 psi, the glass plate deflection is 40 μm while lapping plate deflection is 5.5 μm. The net pad deflection is thus 34.5 μm. Therefore, for the case described in Fig. 7, moderate polishing pressures will be sufficient to initiate contact with the CMOS workpiece.

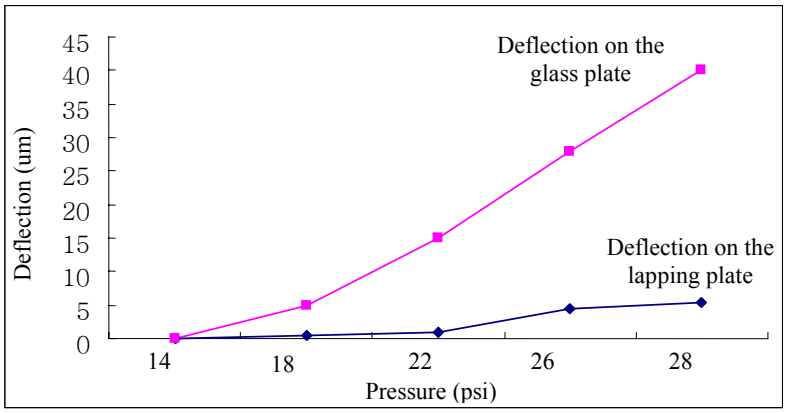


Figure 8. Pad deflection under polishing pressure

The polishing rate for eight silicon dummy pieces was measured when using a 50 nm colloidal silica slurry, pad spindle of 70 rpm, and reciprocating arm spindle of 40 rpm. Two air pressures--20 and 22 psi--were compared for a polishing time of 20 minutes. For the 20 and 22 psi pressures, the polishing rate was 0.13 μm/min and 0.23 μm/min, respectively. Polishing rate depends strongly upon the pressure setting, at least in this range. To compare the polishing rates of silicon and silicon nitride, silicon nitride was deposited on 4 dummy pieces. Four silicon and four silicon nitride dummy pieces were placed in an alternating arrangement on the glass plate and were then polished simultaneously until the average height of the silicon pieces had been reduced by 4 μm. Measurement of the pieces with silicon nitride surfaces showed that they had been reduced in height by only 1.25 to 1.5 μm. We concluded that the polishing rate for the silicon nitride on the CMOS chip is approximately 1/3 times that of the silicon dummy pieces.

A 2.2 μm layer of silicon nitride was sputtered onto a CMOS die, and dummy pieces were prepared to be 1 to 7 μm taller than the CMOS die. After 30 minutes of polishing, an interconnect area was measured with an atomic force

microscope (AFM). The result in Fig. 9 shows that the bumps and via-holes, which are evident in Fig. 3, are barely apparent. The height of the bumps is now less than 25 nm.

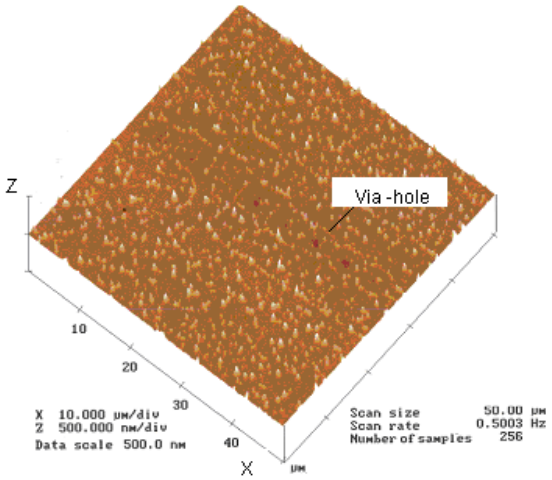


Figure 9. AFM image of the interconnect area after planarization

Measurement with an optical interferometer showed that the peak-to-valley of the curvature profile is 73 nm in the *x* direction and 41 nm in the *y* direction for a 2 mm scan length (see Fig. 10).

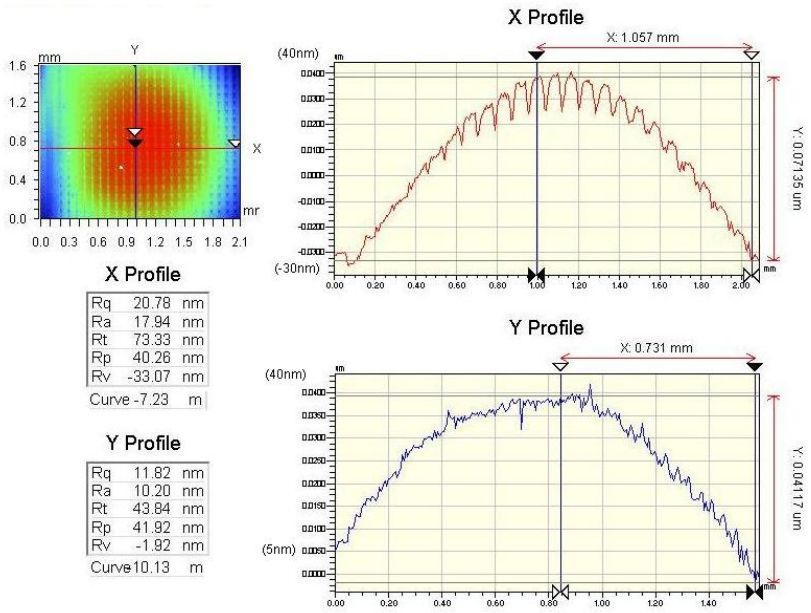
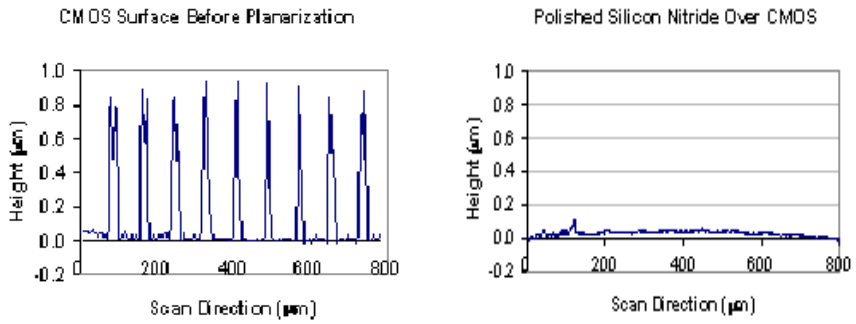


Figure 10. Surface profile of a CMOS die after planarization

Another figure measurement of a CMOS die surface using a stylus profiler is shown in Fig. 11. The polishing process removed the 800 to 900 nm high periodic interconnect bumps. The slightly convex surface that remains is caused by higher local polishing pressures at the die edges.



(a) Before planarization (b) After planarization

Figure 11. Surface profile of a CMOS die before and after planarization

5. CONCLUSION

A planarization method has been developed for preparing small CMOS chips for vertical MEMS integration. Use of chip-size CMOS is especially helpful in the R&D stage of MEMS applications. RF sputtering of silicon nitride at low temperature followed by polishing proved effective in removing 0.9 µm high topography. The polishing process produced a peak-to-valley of the curvature profile of about 70 nm over 2 mm.

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