MEMS spatial light modulators with integrated electronics

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ABSTRACT

The design, fabrication, and preliminary test results of a microelectromechanical, micromachined spatial light modulator (µSLM) with complementary metal-oxide semiconductor (CMOS) electronics, for control of optical phase is presented in this paper. An array of 32 x 32 piston-motion MEMS mirror segments make up the µSLM. Each mirror segment will be capable of altering the phase of reflected light by up to one wavelength for infrared illumination (? = 1.5 µm). The mirror segments are fabricated from metal in a low temperature process allowing for vertical integration of the µSLM with CMOS based, multi-bit, control electronics. The surface of the CMOS is planarized to facilitate µSLM-CMOS integration. The fabrication process and process development results, test results, including frequency response and electromechanical characterization of the (µSLM) actuators, will be presented.

KEYWORDS: spatial light modulator, MEMS, micromirror

1. INTRODUCTION

A spatial light modulator based on full vertical integration of CMOS electronics and surface micromachined piston mirrors is under development at Boston University's Precision Engineering Research Laboratory (PERL). The MEMS devices are fabricated from metal to keep processing temperatures low such that fabrication directly on finished CMOS electronics is possible. Metal micro-mirror devices have been demonstrated in spatial light modulators for phase and/or amplitude modulation [1, 2], as well as integrated with CMOS electronics [3] (Texas Instruments DMD). The micromachined spatial light modulator (µSLM) proposed here will consist of an array of 1024-piston motion MEMS mirror segments fabricated in aluminum over a 3 mm square aperture. Controlled by an underlying 8-bit digital CMOS driver, each pixel will be capable of altering the phase of reflected light by up to one wavelength for visible light, providing a high degree of resolution. Light modulation will be phase-only, with uniform reflected intensity. The mirror elements will be more than 90% reflective and will be optically flat and smooth. The pixels can be closely spaced making a mirror fill factor of 98% achievable for square pixel sizes 100 micrometers on a side. The array will be digitally updated at a rate of 100 kHz.

Fabrication will make use of a low-temperature batch surface-micromachining process integrated with commercially available low-cost foundry electronics fabrication; the device will be economical, reliable and scalable. Figure 1 shows a schematic of nine fully integrated mirror pixels in the proposed µSLM.

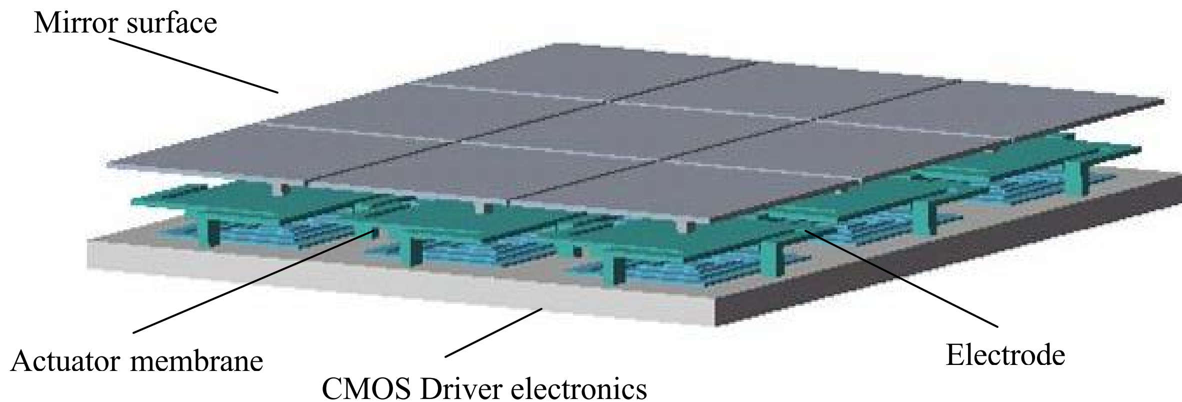


Figure 1. Cross-sectional schematic of three elements in a micro-machined spatial light modulator (µSLM) [2].

In this low temperature MEMS fabrication process, patterned thin layers of structural and sacrificial materials will be built up on a substrate through sequential deposition and lithography. Ultimately, the sacrificial layers will be removed, leaving a self-assembled, integrated opto-electromechanical device. The phase of each individual mirror segment will be controlled by a CMOS data register integrated beneath a parallel-plate electrostatic actuator. The actuation electrode will be divided into concentric rings connected electrically to the underlying CMOS driver. Each ring will have successively larger area, in a geometric sequence, and each will be driven by a binary signal of 0 or 40V. Electrostatic actuation holds considerable promise for SLM shape control because it offers nearly reversible (i.e. low power) actuation, no hysteresis, several micrometers of stroke and nanometer-scale precision and repeatability.

2. BACKGROUND

The low temperature micromachining process is the key to integrating the MEMS devices with CMOS electronics. Metal can be deposited at relatively low temperatures using sputtering and evaporation, each process capable of depositing a smooth film. A key issue in the thin film, however, is the residual stress in the film resulting from the deposition process. This residual stress is partially relieved when the metal MEMS structures are released, resulting in undesired curvature. The two different metal fabrication processes were studied, with an emphasis on defining suitable metal deposition processes and reducing residual strain gradients (and resulting curvature) in thin-film metal structures. DC magnetron sputtering and e-beam evaporation were evaluated as metal deposition techniques. Titanium and aluminum structural materials were tested. The results indicate that DC sputtering of Aluminum offers the most promising approach for development of actuators, primarily because of the wide range of processing conditions available with sputtering and the low annealing temperature of aluminum.

3. ACTUATOR DESIGN AND ELECTROMECHANICAL MODEL

A mathematical model of the proposed actuator was developed to assist in design studies and to predict electromechanical behavior. Figure 3 shows the configuration of the actuator design in which a square membrane is supported by four flexures running parallel to the electrostatic diaphragm of the actuator. In the current design, each individual mirror pixel is actuated electrostatically using electrodes located beneath the square membrane. The mirrors are attached to the actuator by a post attached to the center of the membrane (not shown in figure). The actuator deflection can be determined through a force balance equation between the mechanical restoring force, F_m, and the electrostatic force, F_e establishing an electromechanical equilibrium for the actuator. The mechanical restoring force is

applied to the movable actuator plate through four anchored flexure arms, modeled as fixed-guided cantilever beams; the actuator plate is assumed to be rigid.

$$F_e = F_m \qquad F_e = \frac{\varepsilon A V^2}{2(g-y)^2} \qquad F_m = \frac{4Ewt^3}{L^3} y$$

Where e is the dielectric constant of the actuator gap, V is the voltage applied to the actuator, L is the length of the flexure arm, g is the gap between the actuator diaphragm and the substrate, y is the surface-normal deflection of the actuator plate, E is the modulus of elasticity of the actuator material, w is the width of the flexure arm, and t is the thickness of the flexure arm.

The µSLM design targets are listed in Figure 2 below:

Parameter	Value	Limitation
Max driving voltage, V	40 V	CMOS driver
Required stroke	0.78µm	1/2 ?
Required nat. freq.	100 kHz	SLM specification
Min pixel size	100µm x 100µm	CMOS 8 bit RAM size

Figure 2. µSLM design constraints

The minimum gap size should be three times the required stroke to prevent snap-through from occurring. The maximum membrane actuation area is based on a mirror size of 100 µm x 100 µm and a flexure width, w, of 5 µm. Given these size constraints and the geometry shown in Figure 3, an actuator thickness, t, of 1 µm, and flexure length, L, of 35 µm allow the required stroke with the maximum available voltage. Modeling the actuator/mirror as a simple mass-spring system, this proposed geometry yields a natural frequency of 110 kHz.

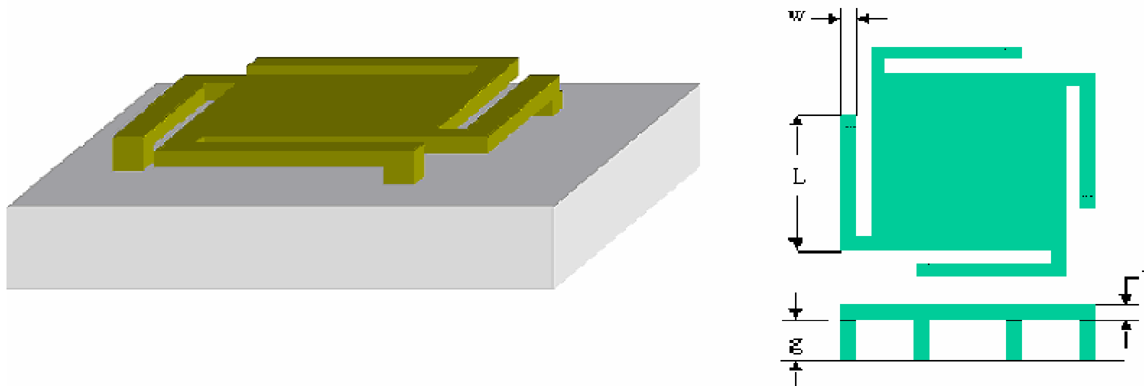


Figure 3. Actuator configuration

4. FABRICATION PROCESS

A fabrication process is under development to produce a metal micro-spatial light modulator (µSLM), which is vertically integrated with complementary metal oxide semiconductor (CMOS) driver electronics. Due to the temperature constraints set by the CMOS, this process must be held to relatively low temperatures (< 150° C) while providing the performance characteristics noted earlier in this paper. Such performance characteristics are attainable and proven using silicon processing [1]. However, Si processing subjects devices to temperatures which exceed the limits of the CMOS.

For this reason, an Aluminum alloy has been chosen. It has been shown to meet the structural requirements as well as the reflectivity requirements established by the project.

To begin, the CMOS chip is planarized to create a flat and smooth base for the mirror components, as excessive topography on this surface would likely print-through to subsequent device layers. Via-cuts are made to connect the contacts on the CMOS chip to the device electrodes. The electrodes are then patterned and metal is deposited on top of the planarized CMOS chip. A sacrificial photoresist layer is applied next, establishing the electrode/actuator gap. This resist layer is patterned with holes which, when the subsequent metal deposition is completed, form the actuator anchors to the substrate. This metal layer is patterned and etched to form the actuator flexures and membrane. A second sacrificial layer is then applied and patterned to form a second, similar array of holes which, when deposited with metal, form the mirror posts. This metal layer is patterned and etched to define the mirror surfaces. Finally, the whole device is released by removing the sacrificial layers, yielding a free-standing, self-assembled MEMS structure. Using this process, arrays of actuators have been fabricated of up to 32 x 32 (1024) mirror pixels. Figure 4 shows a portion of a 32 x 32 array of actuators.

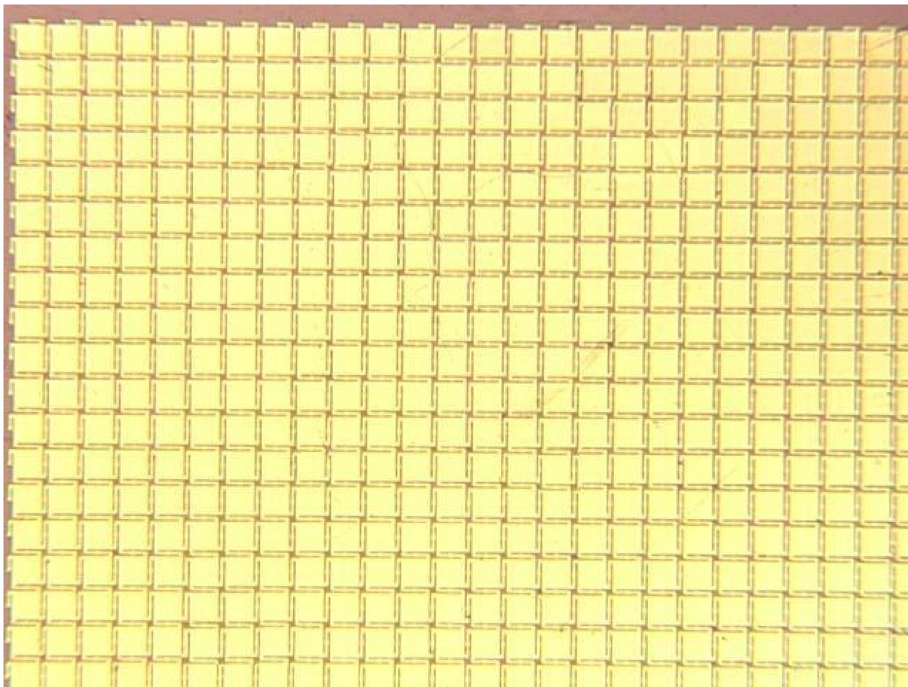


Figure 4. Portion of a 32 x 32 array of actuators.

4.1 Planarization and Via-Cut of CMOS

The planarization and via-cut process has been shown to be effective at providing a smooth, flat surface on which the subsequent device layers can be built. Figure 5 shows an image of the surface topography of the CMOS chip using a WYKO NT2000 3D Optical Surface Profiler. This planarization is accomplished through a multi-step process involving material deposition, chemo-mechanical lapping and polishing (CMP), photolithographic patterning and etching.

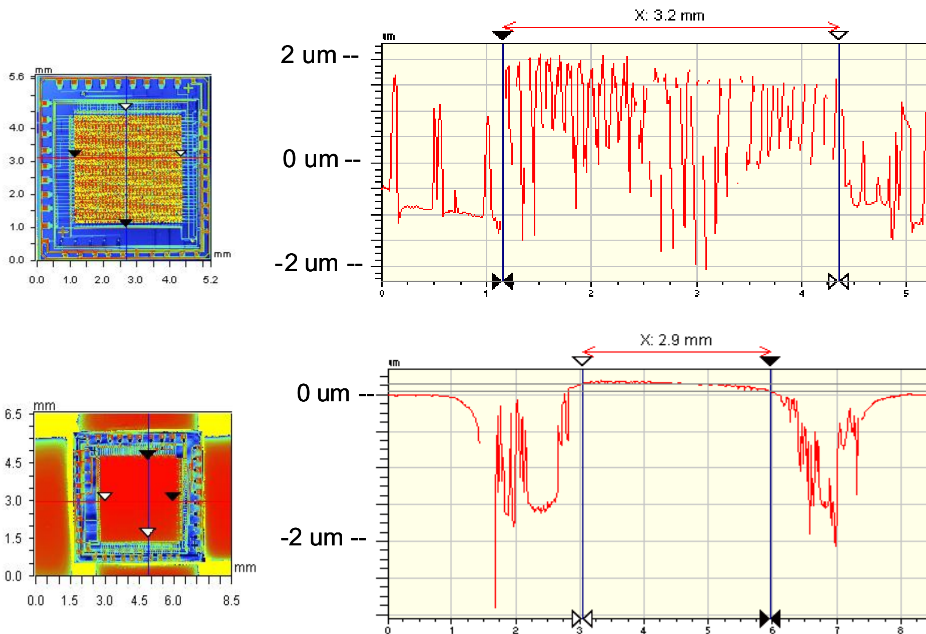
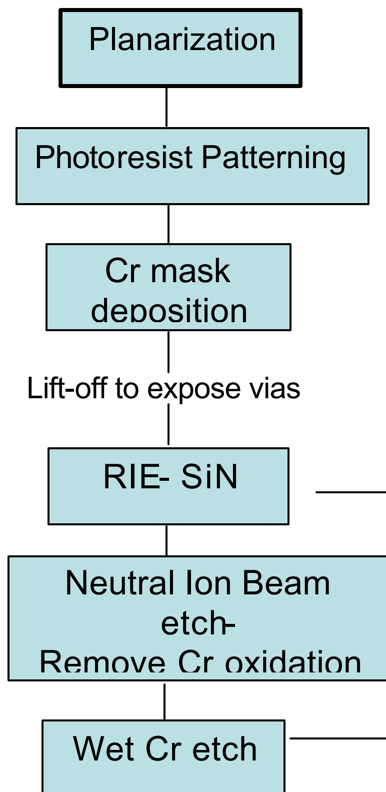


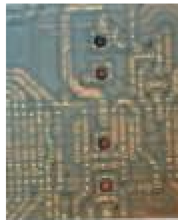
Figure 5. Top image: Before planarization (890 nm RMS roughness).
Bottom image: After planarization (< 30 nm RMS roughness).

First, the chip is cleaned and de-scummed using an O_2 plasma reactive ion etch (RIE) process. Using RF sputtering, 3.3 µm of Silicon Nitride is then deposited as a polishing layer. The chip is adhered to a glass block and surrounded by Si dummy pieces which are lapped to a uniform thickness to control unwanted tilt during the CMP. The chip is then polished, during which surface topography is reduced to less than 30 nm RMS. The chip is then cleaned thoroughly.

In order to make an electrical connection from each contact on the CMOS chip to the surface and eventually the device electrode, a via-cut must be made through the passivation and planarization layers. See Figure 6 for via-cut process flow. This is done by patterning positive photoresist with a bright field mask and using lift-off of a chrome etch stop. RIE is then used to remove the Silicon Nitride and expose the CMOS contacts below, creating the vias. Using a Prism PSM-2000 Neutral Ion Beam machining tool, the Cr oxide layer is removed. A final wet etch step removes the remaining Cr mask.

The chip is then cleaned and is ready for the MEMS device layers to be fashioned on top.





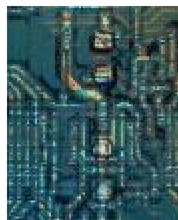


Figure 6. Via-cut process flow.

4.2 Electrode, Actuator and Mirror Fabrication

Eliminating the need for final assembly steps, the MEMS μSLM is fabricated directly on top of the CMOS driver electronics (as shown in Figure 7). A layer of photoresist is applied and patterned to form the concentric square pads which, when metallized, establish an electrical connection to the CMOS driver electronics through the vias formed in the previous step.

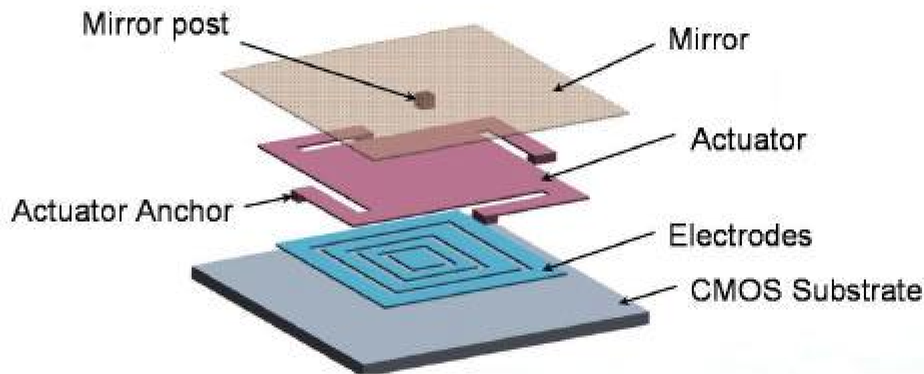


Figure 7. Exploded view of a single pixel. [2]

Using a Denton Discovery 18 DC Magnetron sputtering system, roughly 100 nm of Aluminum alloy is deposited on the substrate. The chip is then immersed in acetone and ultrasonically agitated to lift-off the remaining photoresist as well as the metal above it, leaving just the electrode pattern in metal.

The first sacrificial photoresist layer (PR1) is applied to a thickness of 2.5 μm. This gap size provides the 780 nm of mirror travel required by the project before risking snap-through of the actuator. This resist layer is patterned with 5 μm square holes which, when the subsequent Metal 1 layer is complete, will serve as the actuator anchor posts. This Al alloy layer is now deposited, to a thickness of 800 nm. A photoresist mask layer is now applied and is patterned in the shape of the actuator membranes and flexure arms. This mask pattern is aligned such that the anchors produced in the previous step sit directly beneath the flexure arms so as to maintain the 2.5 μm elevation above the substrate after the (PR1 and eventual PR2) sacrificial layers are removed. Once the actuator mask pattern has been developed, the device undergoes its first of two etch steps. Using the Prism PSM-2000 Neutral Ion Beam machining tool, the Metal 1 layer is etched to reveal the actuator pattern with its supporting anchors. An O_2 plasma RIE de-scum step then removes the actuator mask resist.

In order to fabricate the mirror posts and mirrors on top of the actuators, a process has been developed which is very similar to the one just used to fabricate the anchors and actuators. A second sacrificial photoresist layer (PR2) is applied to a thickness of 2.5 μm. This thickness, and the resulting gap, is not critical to the device performance. Holes are patterned in the resist, similar to the anchors, though these are placed such that one is in the center of each actuator membrane. The Metal 2 Al alloy layer is then sputtered on top of the PR2. The thickness of this layer can be varied as a "tuning" effect to achieve the required 100 kHz natural frequency of the device as set by the project. The 98 μm squares, aligned such that each has a mirror post in the center, are then patterned on the metal as an etch mask. With only 2 μm of space between the mirrors, a fill factor of 98% is achieved, as required by the project. The Prism PSM-2000 Neutral Ion Beam machining tool is once again used to etch the Aluminum Metal 2 layer.

The final fabrication step is to release the structure by removing the sacrificial photoresist layers. This is accomplished using an acetone bath. To prevent stiction, critical point drying (CPD) is utilized.

5. ELECTROMECHANICAL PERFORMANCE

Test structures have been fabricated using slight variations in the above process. Figure 8 shows static voltage versus deflection test results of 5 actuators. The maximum deflection was 715 nm at 53 volts, as measured interferometrically at the center of the actuator using the WYKO NT2000 3D Optical Surface Profiler. This tool has a measurement repeatability of about 20 nm.

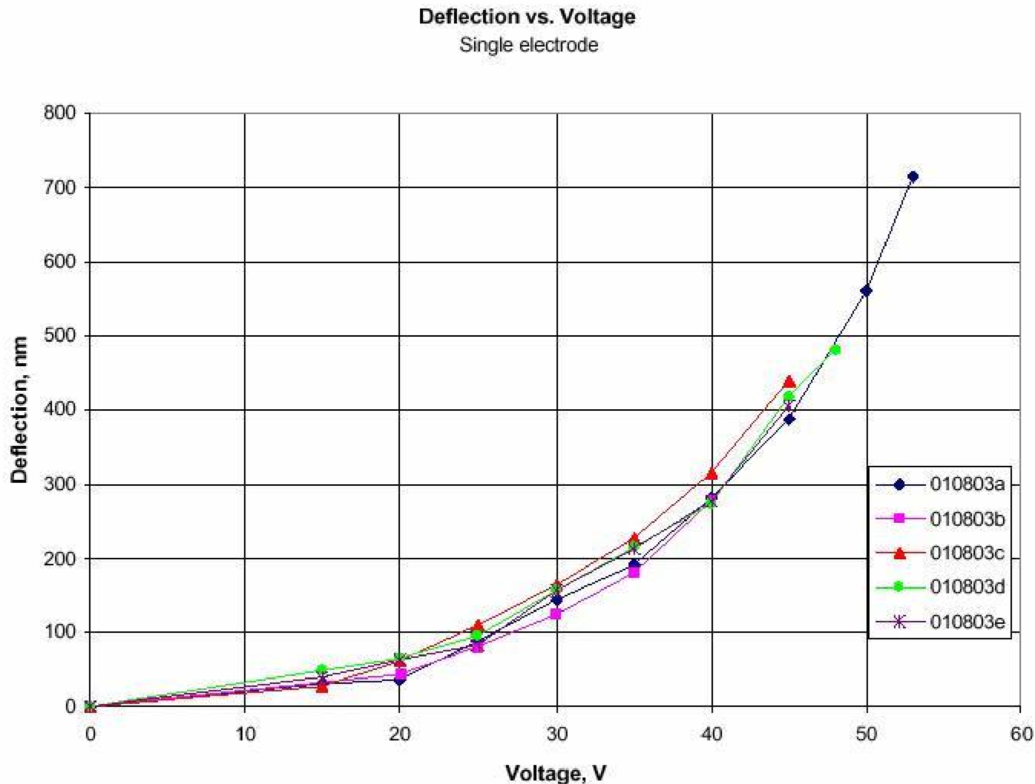


Figure 8. Deflection vs. Voltage for 5 actuators. [2]

These actuators have one large electrode instead of the split electrodes used in the actual device. The stiffness of these actuators is approximately 16 % less than the theoretical value. This is attributed to the fact that the boundary conditions are not ideal as assumed in the theoretical analysis.

Dynamic testing has also been accomplished using similar single electrode actuators to the ones whose static deflection data was just presented. The natural frequency requirement set by the project is 100 kHz. Early test results, using a Zygo ZMI-1000 laser interferometer, have yielded a natural frequency of 60 kHz. The natural frequency of the device can be "tuned" using small changes in the film thickness of the mirror as well as other small changes in the actuator flexure design.

6. CHALLENGES

Research is ongoing to find a repeatable Aluminum alloy deposition process which will yield consistently flat actuators and mirrors. When the film is deposited, it is constrained by the layer below. In this case, it is the sacrificial photoresist layer to which it is adhered. Whatever stress exists in the material will be relieved once the structure is released. Thus, in a two layer system, a more tensile stress on the first layer with a more compressive stress on the second layer will result

in a film which is concave-down when released (and concave-up for a film with a more compressive stress deposited first and a more tensile stress deposited second). See Figure 9.

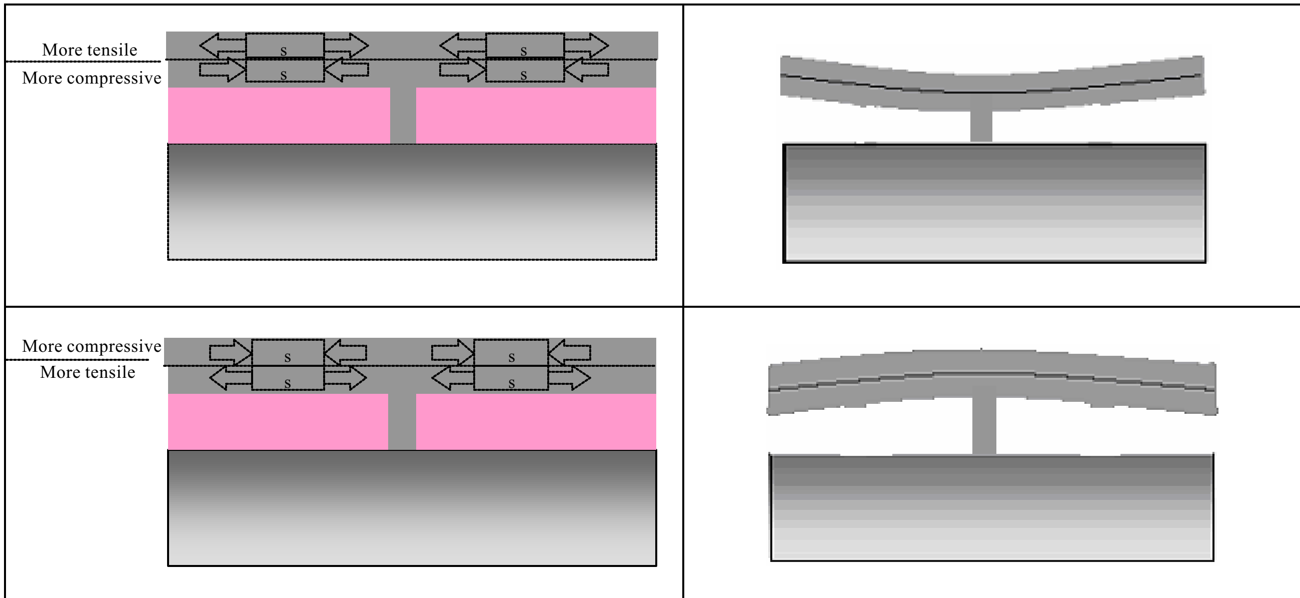


Figure 9. Left: Stress gradient profile prior to release. Right: Stress relieved after release.

Current effort is centered about substrate temperature control as a means by which stress gradients can be reduced. Temperature measurement testing was done using a thermocouple placed on a Silicon chip on the standard chuck in the Denton DC Magnetron sputterer. Different Argon partial pressures and sputter powers were plotted to see the heating and cooling profile. The most significant results are shown in Figure 10.

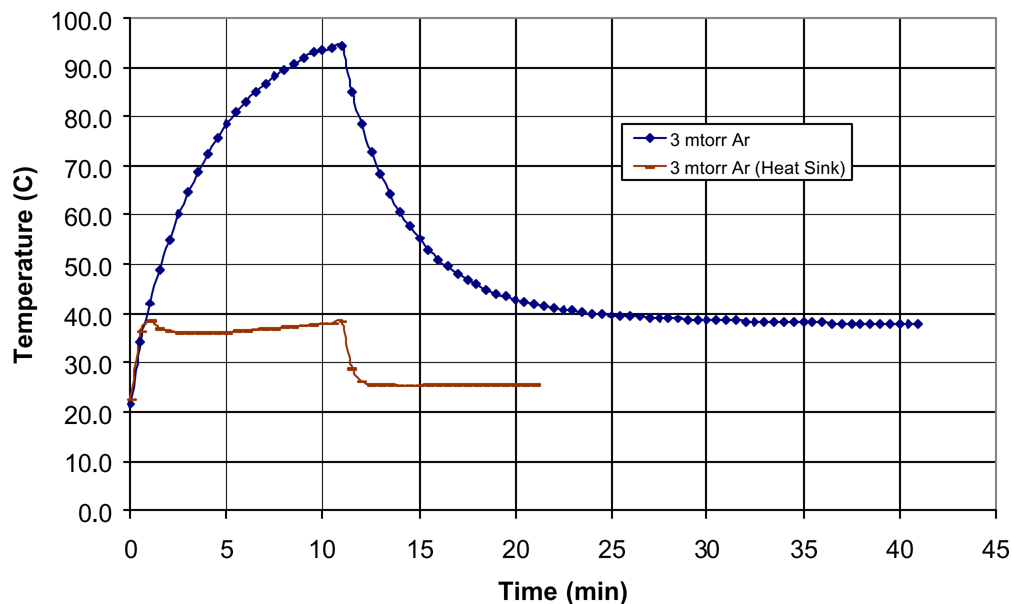


Figure 10. Substrate temperature in DC Magnetron sputterer.

This temperature gradient alone is the cause of a great deal of stress, as given by the equation relating Coefficient of Thermal Expansion (CTE) to stress:

$$\sigma = E\frac{\alpha \Delta T}{L}$$

where a is the CTE, ?T is the change in temperature, L is the original length and E is the Modulus of Elasticity of the Al alloy. Any reduction of the slope of this heating curve would help to reduce the stress gradient in the film. The second curve shows the result of the sample being placed on a thick copper block (which was shielded from the plasma). This copper block acted as a heat sink, allowing for an increase in temperature upon first exposure to the plasma, but then settling down to a small rise over the majority of the 11 minute sputtering period. This heat sink, however, could only provide a damping effect on the substrate temperature. For full control of the deposition temperature, a new chuck, shown in Figure 11, needed to be fabricated.

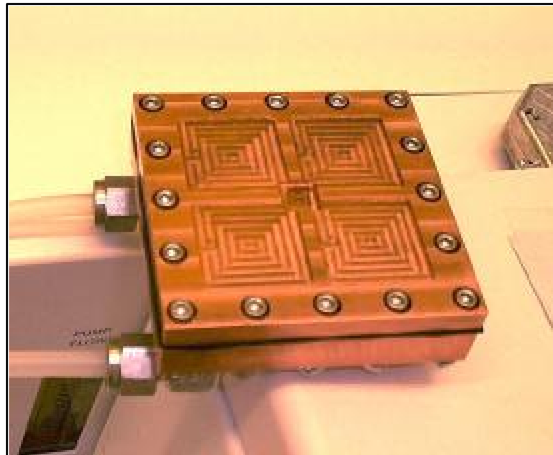


Figure 11. Copper temperature control chuck for use in DC Magnetron sputterer

A temperature control chuck for use in the Denton Discovery 18 DC Magnetron sputterer has been designed and fabricated at the Precision Engineering Research Laboratory at Boston University. The standard chuck in the tool has been replaced by this two-piece copper chuck, which uses machined internal water jackets to circulate heating or cooling water fed into the chamber through vacuum rated pass-throughs from a heater/chiller on the outside. The Neslab RTE-134 Heater/Chiller which has a temperature range of 5° C to 35° C will be used.

A two stage deposition process will be performed. The variables during the deposition process will the length of deposition (i.e. thickness of the layer) and the temperature of the substrate during deposition. The metric in which the tests will be measured is the curvature of the released structures.

7. FUTURE WORK

A project milestone in the near future includes establishing a repeatable deposition process to achieve flat actuators and mirrors (< 30 nm RMS). In parallel, a fabrication process for integrating mirrors with actuators is being developed. Work is also ongoing to integrate large actuator arrays with the CMOS driver, leading ultimately to an actuator and mirror device which is fully integrated with and operational on the underlying CMOS driver electronics.

8. REFERENCES

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