

# Ultra-low-power multiplexed electronic driver for high resolution deformable mirror systems

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## ABSTRACT

We present a new multiplexed high-voltage driver architecture that departs from previous MEMS deformable-mirror drivers. Just one D/A converter and one high-voltage amplifier module drive the entire actuator array through a row-column addressing scheme. This approach reduces operational power consumption of a multiple-channel deformable-mirror driver by two orders of magnitude. It can provide for the integration of the deformable mirror and driver into a compact package, reducing driver volume by an order of magnitude. Both of these system modifications are essential for the implementation of MEMS deformable mirrors into space-based adaptive optics systems and other applications.

**Keywords:** actuator, driver, high-voltage, multiplexer, low power, MEMS

## INTRODUCTION

Electrostatically-actuated deformable mirrors fabricated using MEMS techniques provide a compelling and intrinsically advantageous approach to adaptive optics. Compared to other kinds of wavefront controllers, a MEMS deformable mirror (DM) offers reduced size, weight, and power consumption. These chip-scale, thin-film silicon devices are capable of more than a thousand optical degrees of freedom [1-14]. The diagram of Figure 1 depicts a DM structure used for adaptive optics. The mirror surface is supported by a multitude of MEMS actuators each capable of motion perpendicular to the plane of the mirror. By separately adjusting the displacement of each actuator, the precise shape of the mirror surface can be controlled. Deformable mirror technology has progressed to the point where a 1-cm size DM may contain several thousand actuators. Each of the latter requires its own analog driving voltage. Small-stroke ( $\sim 1 \mu\text{m}$ ), high-precision DMs scalable to  $10^4$  actuators represent the current state of the art. These devices have numerous applications in medical imaging, space exploration, and other fields of technology. High-resolution wavefront-correcting mirrors are essential, for example, in the telescope architectures proposed as part of NASA's ongoing search for life on extrasolar planets [15,16].

One drawback of MEMS DMs is that the actuators require voltages as high as 300 V to achieve the full stroke needed to properly position the mirror segments. In all commercially available systems now available, each actuator in the array is driven by its own high-voltage (HV) amplifier that converts a digitally-derived, low-voltage signal into the high voltage needed to drive the actuator. Because large numbers of HV amplifiers are needed, DM drivers often represent the primary power demand and cost of MEMS DM adaptive-optics (AO) systems. While ground-based applications are not necessarily limited by a DM driver's power consumption or compactness, the sheer number of high-voltage amplifiers needed for a  $10^4$ -element array would require an entire cabinet rack and a prohibitive amount of quiescent power. For currently planned and future space-based applications, both power and size become critical limitations.

### 1. Solving the many-amplifier problem

One solution to this problem is a multiplexing circuit fed by single HV amplifier. The multiplexer distributes the HV amplifier output sequentially to each actuator in the array. Because only a single amplifier is used, both quiescent power and overall cost are reduced dramatically. We have developed the prototype of such a system that can drive 144 actuators at a refresh rate of 10 ms. Each multiplexer output can produce up to 300 V with a resolution of 3 mV, consistent with 16-bit (1 part in  $2^{16}$ ) digital conversion. Compared to a conventional, one-amplifier-per-actuator system,

our system reduces power consumption by a factor of about 100, to a level of just a few hundred milliwatts. Moreover, the circuit architecture is fully scaleable to an arbitrarily large number of actuators.

### 1.1 MEMS Actuator electromechanical behavior

The electro-mechanics of MEMS actuators has been covered extensively in the literature and will be summarized only briefly here. To first-order, an actuator can be modeled as a parallel-electrode capacitor with one electrode fixed and another supported by a linear spring having restoring force constant  $k$ , as in Figure 1. The typical actuator in a MEMS optical DM has a lateral width on the order of  $300\ \mu\text{m}$  and a zero-voltage gap spacing  $g$  of about  $5\ \mu\text{m}$ . These dimensions result in an actuator capacitance of about  $160\ \text{fF}$ . The voltage applied between the electrodes determines the electrostatic force, and hence the displacement  $y$  of the moving electrode. When a voltage  $V$  is applied, attractive electrical and restorative mechanical forces balance, yielding the well-known displacement versus voltage equation:

$$\frac{\epsilon_0 L w V^2}{2(g - y)^2} = ky \tag{1}$$

The resulting displacement depends on the square of the voltage, and thus is polarity independent. By adjusting the voltage of each actuator in the array, the optical contour of the mirror that is supported by the actuators can be precisely controlled.

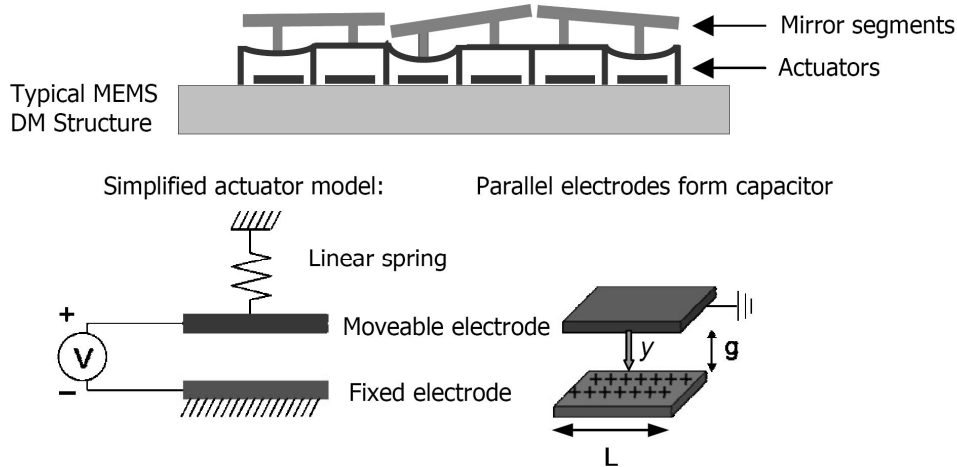


Figure 1. Simplified spring-capacitor model for a MEMS actuator

### 1.2 High-voltage multiplexer concept

While one-to-many multiplexing schemes are commonplace in low-voltage electronics, we believe that a MEMS-array driving system based on a single D/A converter and a single high-voltage amplifier to be innovative. The basic architecture for such a system is depicted in Figure 2. It consists of an  $n$ -bit digital bus, a low-voltage D/A converter, and one high-voltage amplifier. Each actuator is connected, in turn, to the output of the amplifier by its own, separate driving cell. The latter is addressed by logic-level (e.g.,  $3.3\ \text{V}$ ) row- and column-line signals. Over a repeating refresh cycle, the system addresses each actuator cell in turn. When its cell is selected, an actuator is momentarily connected to the output of the high-voltage amplifier. Thereafter, the actuator's driving cell holds its voltage until the next refresh event. For this purpose, a holding capacitor, much larger than the actuator's tiny  $150\text{-fF}$  capacitance, is connected in parallel. This capacitive-storage mode resembles that used in low-voltage dynamic memory devices (DRAM).

The overall precision of the controller depends on the noise floor of the HV amplifier, the “droop” of the holding capacitor's voltage between refresh cycles, the array refresh rate, and the precision of the D/A converter. One advantage of using a large holding capacitor for each cell is that it inherently filters and reduces amplifier noise, in essence adding a low-pass filter to each driver channel.

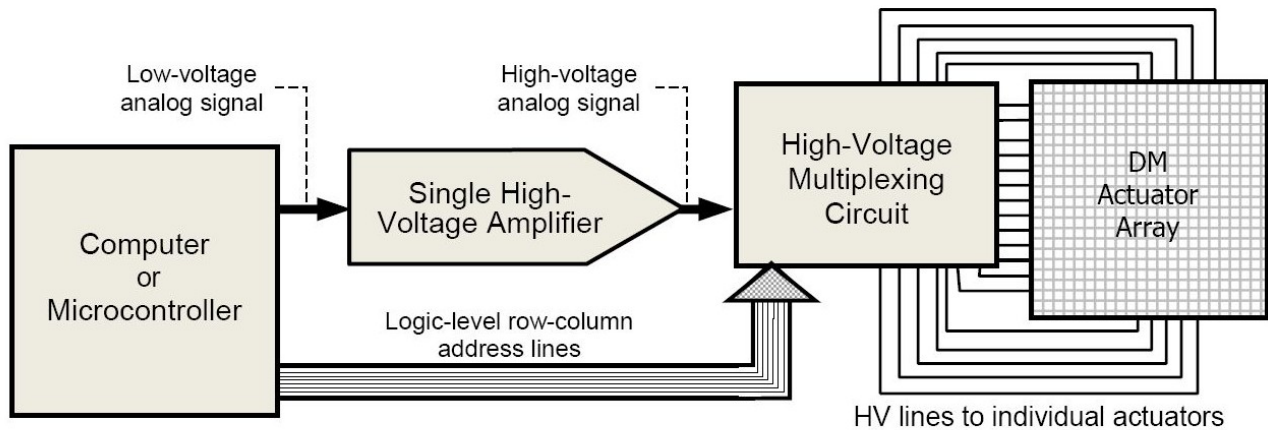


Figure 2. Block diagram of multiplexer circuit architecture. Low-voltage logic lines control the conduction state of high-voltage transistors that couple or isolate high-voltage signals to the DM actuators

## 1.2 First attempt at driver cell design

Designing a high-voltage analog multiplexer presents several challenges, the main one being the interface between the logic-level row and column voltages and the high voltage signals needed to drive the actuators. At first glance, the circuit scheme of Figure 3 seems the obvious choice, and is the first architecture that we tried. It comprises a single, current-driven, high-voltage bipolar transistor (PNP BJT) used as a switch. Logic-level MOSFETs monitor the row and column address lines. The BJT connects the output of HV amplifier to the actuator when it's cell is addressed. In preliminary work, a low-voltage version of this circuit was successfully tested to demonstrate feasibility. When we attempted to transition the design to high actuator voltages (~250 - 300 V), however, a significant problem emerged.

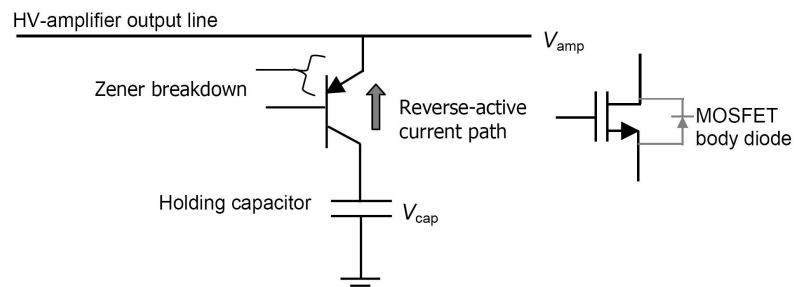


Figure 3. Illustration of problem with single-transistor switching approach. When  $V_{cap} > V_{amp}$ , the capacitor discharges to the voltage of the HV-amplifier output via reverse-active conduction of the bipolar-junction transistor in conjunction with zener breakdown of the transistor's base-emitter junction

Each cell has the job of connecting its holding capacitor to the HV amplifier output once per refresh cycle. When the PNP BJT in Figure 3 is activated, it saturates, charging the holding capacitor to within a saturation voltage (about 0.2 V) of the HV signal line. (Because most DM applications require precision and repeatability, but not absolute accuracy, a fixed saturation voltage drop is fully tolerable.)

The circuit of Figure 3 works well for the case where the output of the HV amplifier lies above the voltage of the cell's holding capacitor. If the capacitor is charged to a particular voltage, however, and the HV amplifier output subsequently falls below that voltage – for example, in preparation for addressing the next cell in the array – the capacitor of the cell with the higher voltage immediately discharges to the lower value of the HV amplifier output. In other words, a given holding capacitor cannot hold any voltage higher than the instantaneous value of the HV signal line.

Upon reflection, we were able to explain this behavior by considering the “reverse-active mode” of bipolar transistors [17,18]. A PNP bipolar transistor has a small-area, *p*-type emitter region, a thin *n*-type base, and a *p*-type collector of larger area. The large collector/emitter area ratio is responsible, in part, for the large current gain of the transistor. Under

normal (forward-active) operation, the emitter is more positive than the collector, and current flows from the former to the latter when an external circuit forward biases the base-emitter junction. In the case where the collector is more positive than the emitter, as occurs in Fig. 3 when the cell's storage capacitor is charged to a higher voltage than HV signal line, then the transistor is capable of conduction from the *p*-type collector to the *p*-type emitter. Conduction in this "reverse-active" mode occurs at much lower current gain (e.g., a  $\beta$  of 2 rather than about 100), but the resulting current is sufficient to discharge the holding capacitor to the lower voltage of the HV signal line.

Exacerbating the problem is the zener effect, whereby the base-emitter junction of a BJT breaks down at a relatively small voltage (on the order of 10 V) [17,18]. This breakdown occurs because the emitter is very highly doped in comparison to the base (a necessary condition for high forward-active current gain). This high doping causes avalanche breakdown when the base-emitter junction is reverse biased to excess. In low-voltage circuits, these combined phenomena are of little consequence. In a high-voltage circuit, such as the one of Figure 3, the zener voltage of the base-emitter junction is easily reached, hence the combined effects act to discharge every holding capacitor to the lowest occurring voltage of the HV signal line.

Replacing the PNP BJT with a high-voltage MOSFET leads to a similar situation. As is well known, all MOSFETs contain an internal body diode, shown in Figure 3, that is intrinsic to the MOS fabrication process. This diode remains reverse biased at all times when the drain (for an NMOS) is more positive than the source. In our circuit configuration, however, this condition cannot be maintained, because the HV signal line will always fall below the drain voltage of some of the MOSFETs in the array. Under these conditions, the MOSFETs body diodes similarly discharge all holding capacitors to the lowest occurring voltage of the HV signal line.

### 1.3 Second attempt at driver cell design

A solution to the aforementioned problem can be found in the circuit of Figure 4. Logic-level row and column address signals control the on/off states of MOSFETs  $M_1$  and  $M_2$ . These devices drive a network of high-voltage bipolar transistors (BJTs) which connect the HV amplifier output to the cell's actuator and holding capacitor when both MOSFETs are "on". During the remainder of the refresh cycle, both MOSFETs are never on simultaneously (i.e., the cell is not addressed), causing the BJT network to retain a high-impedance state between its holding capacitor and the HV amplifier output. Notably, this high impedance can sustain voltage polarity in either direction, thereby allowing a given cell to retain its assigned analog voltage for the duration of the refresh cycle, including times when the HV signal line lies at a lower voltage/

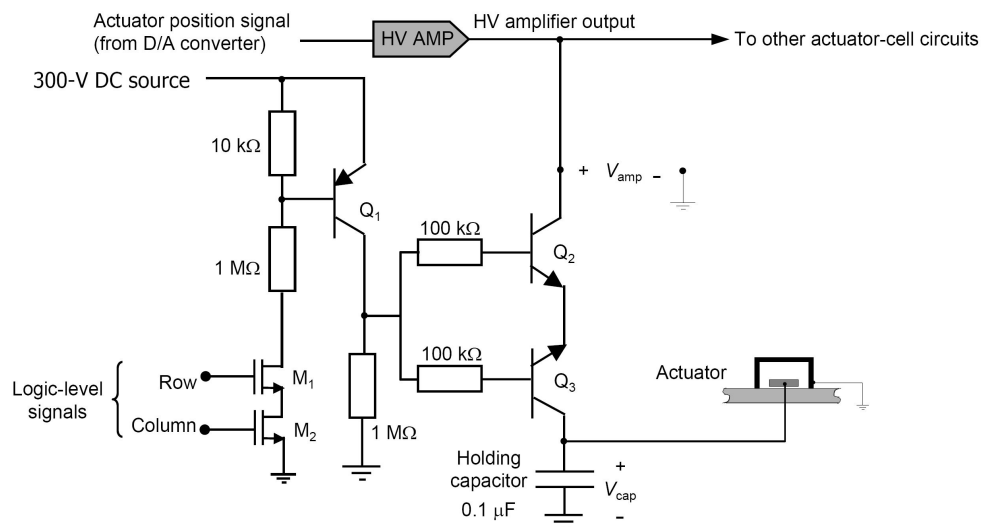


Figure 4. Actuator cell circuit. Logic-level row/column signals activate  $Q_1$  which causes  $Q_2$  and  $Q_3$  to connect the holding capacitor to the HV-amplifier output. With  $M_1$  or  $M_2$  off, the holding capacitor is disconnected regardless of the relative values of  $V_{cap}$  and  $V_{amp}$ . Transistor types as follows:  $Q_1 = ZTX657$ ;  $Q_2$  and  $Q_3 = ZTX757$ ;  $M_1$  and  $M_2 = ZVN0545$

The circuit of Figure 4 intentionally utilizes the reverse-active BJT mode to advantage. When both the cell's row and column MOSFETs are activated, the PNP transistor  $Q_1$  closes, causing current to flow from the fixed DC source to the bases of the NPN transistors  $Q_2$  and  $Q_3$ . The latter are connected in series between the holding capacitor and the HV amplifier output. It is important that the voltage of the DC source be higher than the highest possible output of the HV amplifier.

When the cell is addressed, either  $Q_2$  or  $Q_3$  will conduct in the forward-active mode; the other of the two will conduct in the reverse-active mode, thereby completing the current path between holding capacitor and analog signal line.. Which transistor conducts in which mode will depend of the relative values of  $V_{cap}$  and  $V_{amp}$ . Which BJT receives base current will depend on the relative voltage levels of the capacitor and the HV signal line.

For example, when  $V_{amp}$  exceeds  $V_{cap}$ , transistor  $Q_2$  will saturate the forward-active mode, and  $Q_3$  will saturate in the reverse-active mode, thereby connecting the HV amplifier output to the holding capacitor. Conversely, when  $V_{cap}$  exceeds  $V_{amp}$ , the opposite occurs:  $Q_2$  and  $Q_3$  and will conduct in the reverse-active and forward-active modes, respectfully.

With either or both MOSFETs off (cell not addressed),  $Q_1$  ceases to conduct, thus preventing base current from flowing to  $Q_2$  and  $Q_3$ . The connection from the holding capacitor to the HV-amplifier output is broken and replaced with a high-impedance path. Although one base-emitter junction of  $Q_2$  and  $Q_3$  may go into zener breakdown, the other will remain in proper forward polarity, thereby sustaining the high-impedance pathway up to the voltage rating of  $Q_2$  and  $Q_3$ .

## 2. ARRAY PERFORMANCE

Using the cell circuit of Figure 4, we built a 144-channel prototype of the system, shown in Figure 5. A Texas Instruments TI-MSPF2619 microcontroller with on-chip, 12-bit, D/A converter provided the needed digital control and analog-to-digital conversion. Performance of the actuator holding-capacitor cell architecture was verified by measuring per-channel noise level, position stability, capacitor-voltage "droop" (decay between refresh cycles), and total array power consumption. The multiplexer updates the voltage of each actuator every 10 ms (e.g., a 100-Hz refresh cycle). The duration of the update interval is 60  $\mu$ s for each actuator cell. One figure of merit of the apparatus is its ability to minimize change in actuator voltage between refresh cycles. The main component of this variation, capacitor voltage droop, must be held within tolerance over the 10-ms duration of the refresh cycle.



Figure 5. 144-channel prototype of a high-voltage MEMS array driver

### 2.1 Position stability and droop

NASA, the sponsor of this project\*, has a demanding application for a low-power, spaced-based DM system requiring each actuator to hold its position to a precision of about 10 picometers over a stroke range of 1  $\mu$ m. As noted above, the precision of each actuator is limited by the effect of charge leakage from the holding capacitor between refresh cycles. Typically, drift is associated with an impedance path to ground that allows the stored capacitor charge to dissipate.

The uniformity of the driver output voltages and the droop characteristics for the 144-cell DM driver of Figure 4 were tested by connecting the multiplexer to a micromirror array and making displacement measurements using a Zygo

NewView optical surface-mapping profilometer. Although the resolution of this white-light scanning phase-shift-interference microscope is only about 1 nm, mirror profile changes associated with actuator position, as altered by capacitor droop, were interpolated to a precision of 1 pm. The latter was accomplished by measuring actuator displacement over a large time interval (seconds), then interpolating the result to the 10-ms duration of the refresh cycle. This extrapolation assumes that droop occurs at a constant rate, which our data show to be approximately true.

In the droop evaluation experiment, all of the 144 actuators in our segmented DM were simultaneously row-column selected and pre-charged to an initial voltage of 100 V. All cells were then un-addressed, and their holding-capacitor voltages on allowed to decay. The mirror segment positions associated with the decaying voltage were simultaneously measured on some representative cells using the Zygo instrument. Both capacitor voltage and displacement variation were measured every 10 s over a time span of 10 min.

The droop rate of the actuators we tested resulted in position drift rates ranging between 0.32 nm/s and 4.39 nm/s. The worst-case droop result, showing displacement drift-versus-time, is shown in Figure 6. The aforementioned drift rates were interpolated based the initial slope of the drift versus time plots. The variations in droop performance are likely linked to variations in leakage-path resistance from cell to cell in the micromirror array, as well as to the tolerances selected for the off-the-shelf driver components, the latter of which also produce some variability in the targeted voltage map. We note that in a working system, these variations can be easily calibrated and compensated for by the controlling microprocessor. In any case, the measured drift values suggest that, over the 10 ms/frame refresh rate of the controller, drift can be held to 5 pm, even for the worst case. While these results are encouraging, motion repeatability and stability will need to be measured in future experiments.

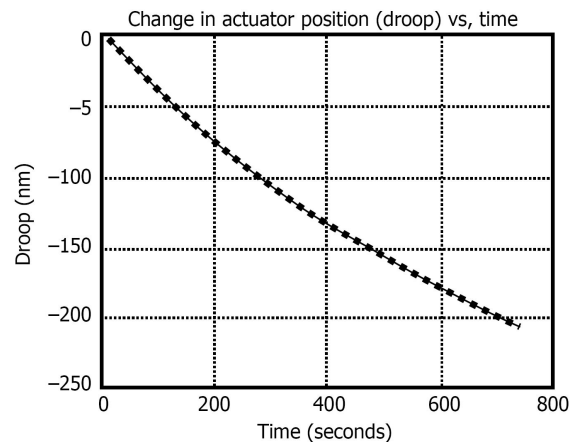


Figure 6. Plot versus time of change in actuator position due to droop in holding capacitor voltage

## 2.2 Power Consumption

Two different experiments evaluated power consumption of the driver prototype. In the first, designated the “low power test”, each channel of the driver was precharged to 150 V. Its voltage was then switched by  $\pm 1$  V every 10 ms (i.e. at the frame refresh rate). Average power consumption values were separately measured for the microcontroller, high-voltage DC power supply, and HV analog amplifier. In the second experiment, designated the “high power test”, each channel of the driver was switched between 0 V and 150 V over each refresh cycle, thus providing maximum cyclic excursion for each actuator. The results of both tests are shown in Table 1.

The low-power experiment, in which the total power consumption was about 150 mW, corresponds most closely to the anticipated operating conditions of a space-based coronagraph instrument for which NASA may use our system. In such an application, only small corrections to mirror profiles need be made each refresh cycle. These minor voltage adjustments – on the order of millivolts -- compensate for slowly varying, thermally-driven, picometer-scale changes in mirror profile. A mirror installed as part of a coronagraph telescope structure would require only small perturbations in DM shape over each refresh cycle.

**TABLE 1: POWER CONSUMPTION IN THE 144-CHANNEL PROTOTYPE DRIVER**

<u>Component</u>	<u>Low Power Test (typical use)</u>		<u>High-Power Test (extreme use)</u>	
Microcontroller (3.3 V)	25 mW	(3.3 V × 7.6 mA)	25 mW	(3.3 V × 7.6 mA)
DC Power Supply	22.5 mW	(250 V × 90 μA)	32.5 mW	(250 V × 0.13 mA)
High-Voltage Amplifier:				
Quiescent Power (no capacitors being charged)	100 mW	(250 V × 0.4 mA)	100 mW	(250 V × 0.4 mA)
Additional Output Load (capacitor charging intervals)	4.5 mW	(150 V × 30 μA)	600 mW	(150 V × 4 mA)
Total Power	152 mW		758 mW	

## CONCLUSION

We have built and tested a 144-cell prototype for a fully scalable, multiplexed, high-voltage driver system for a multi-channel MEMS mirror array. The architecture represents a significant departure from MEMS mirror drivers now in use. A single D/A converter and a single high-voltage amplifier drive the entire actuator array through a row-column addressing scheme and an array of high-voltage switching cells, made from bipolar transistors, that includes a holding capacitor connected in parallel with each actuator. One bipolar transistor operates in the reverse-active mode when charging the holding capacitor. The approach reduces operational power consumption two orders of magnitude over conventional designs and can hold the positions of 1 micron stroke actuators to within 5 pico-meters over a 10-ms refresh rate.

The average working power consumption for the 144 actuator system was about 150 mW which falls within the scope of to the anticipated operating conditions for space-based coronagraph instrument and other applications in which NASA has interest. In such an applications, only small corrections to mirror profiles need be made each refresh cycle. These minor voltage adjustments, which are on the order of millivolts, compensate for slowly varying, thermally-driven, picometer-scale changes in mirror profile. A mirror installed as part of a coronagraph telescope structure, for example, would require only small perturbations in mirror shape over each refresh cycle.

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## REFERENCES

- [1] Bifano, TG, Bierden P, Cornelissen SA, "MEMS deformable mirrors for space and defense applications," *Micro (MEMS) and Nanotechnologies for Space, Defense, and Security II*, Orlando, FL, USA, SPIE, [6959], 695914-695917, (2008)
- [2] Bifano T, "Shaping light: MOEMS deformable mirrors for microscopes and telescopes," *MEMS Adaptive Optics IV*, San Francisco, California, USA, SPIE, [7595], 759502-759508, (2010).
- [3] Stewart JB, Bifano TG, Cornelissen S, Bierden P, Levine BM, Cook T, "Design and development of a 331-segment tip-tilt-piston mirror array for space-based adaptive optics," *Sensors and Actuators a-Physical*, [138], 230-238, (2007).
- [4] Cornelissen SA, Bierden PA, Bifano TG, "A 4096 element continuous facesheet MEMS deformable mirror for high-contrast imaging," *MEMS Adaptive Optics II*, San Jose, CA, USA, SPIE, [6888], 68880V-68810, (2008).
- [5] Bifano T, "Shaping light: MOEMS deformable mirrors for microscopes and telescopes," *MEMS Adaptive Optics IV*, San Francisco, California, USA, SPIE, [7595], 759502-759508, (2010).
- [6] Bifano TG, Bierden P, Cornelissen SA, "MEMS deformable mirrors for space and defense applications," *Micro (MEMS) and Nanotechnologies for Space, Defense, and Security II*, Orlando, FL, USA, SPIE, [6959], 695914-695917, (2008).

- [7] Bifano TG, Mali RK, Dorton JK, Perreault J, Vandelli N, Horenstein MN, Castanon DA, "Continuous-membrane surface-micromachined silicon deformable mirror," *Optical Engineering*, [36], 1354-1360, (1997).
- [8] Bifano TG, Perreault J, Mali RK, Horenstein MN, "Microelectromechanical deformable mirrors," *Journal of Selected Topics in Quantum Electronics*, [5], 83-89, (1999).
- [9] Cornelissen SA, Bierden PA, Bifano TG, Lam CV, "4096-element continuous face-sheet MEMS deformable mirror for high-contrast imaging," *Journal of Micro/Nanolithography, MEMS and MOEMS*, 8, 031308-031308, (2009).
- [10] Horenstein MN, Bifano TG, Mali RK, Vandelli N, "Electrostatic effects in micromachined actuators for adaptive optics," *Journal of Electrostatics*, [42], 69-81, (1997).
- [11] Mali RK, Bifano TG, Vandelli N, Horenstein MN, "Development of microelectromechanical deformable mirrors for phase modulation of light," *Optical Engineering*, [36], 542-548, (1997).
- [12] Perreault JA, Bifano TG, Levine BM, Horenstein MN, "Adaptive optic correction using microelectromechanical deformable mirrors," *Optical Engineering*, [41], 561-566, (2002).
- [13] Stewart JB, Diouf A, Zhou YP, Bifano TG, "Open-loop control of a MEMS deformable mirror for large-amplitude wavefront control," *Journal of the Optical Society of America a-Optics Image Science and Vision*, [24], 3827-3833, (2007).
- [14] Stewart JB, Bifano TG, Cornelissen S, Bierden P, Levine BM, Cook T, "Design and development of a 331-segment tip-tilt-piston mirror array for space-based adaptive optics," *Sensors and Actuators a-Physical*, [138], 230-238, (2007).
- [15] <http://planetquest.jpl.nasa.gov/>
- [16] Earth-like exoplanets: the science of nasa's navigator program, JPL Publication 06-5, Rev A (2006)
- [17] Horenstein, MN [Microelectronic Circuits and Devices, 2nd Ed.], Prentice-Hall, Upper Saddle River, NJ, 905-906, (1996).
- [18] Sedra, AS and Smith, KC [Microelectronic Circuits, 4th Ed.], Oxford Univ. Press, New York & Oxford, 305-306 (1998).