Design and fabrication of reflective spatial light modulators for high-dynamic-range wavefront control

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1. ABSTRACT

This paper describes design and fabrication of a microelectromechanical metal spatial light modulator (SLM) integrated with complementary metal-oxide semiconductor (CMOS) electronics, for high-dynamic-range wavefront control. The metal SLM consists of a large array of piston-motion MEMS mirror segments (pixels) which can deflect up to 0.78 µm each. Both 32x32 and 150x150 arrays of the actuators (1024 and 22500 elements respectively) were fabricated onto the CMOS driver electronics and individual pixels were addressed. A new process has been developed to reduce the topography during the metal MEMS processing to fabricate mirror pixels with improved optical quality.

KEYWORDS: spatial light modulator, MEMS, micromirror

2. INTRODUCTION

The development of the new spatial light modulator at Boston Micromachines Corp and Boston University's Precision Engineering Research Laboratory is based on full vertical integration of CMOS electronics and surface micromachined piston mirrors. The micromachined spatial light modulator (µSLM) consists of an array of 1024 or 22500 piston motion MEMS mirror segments fabricated in aluminum. The mirror pixels are closely spaced squares of 100 microns by 100 microns, and mirror fill factor of 98% can be achieved. Controlled by an underlying CMOS driver, each pixel is capable of altering the phase of reflected light digitally by up to one wavelength for visible light. The reflectivity of mirror elements is higher than 90%, the flatness of the mirror pixels is < 30nm RMS, and the update rate of the mirror array will be at 100 kHz.

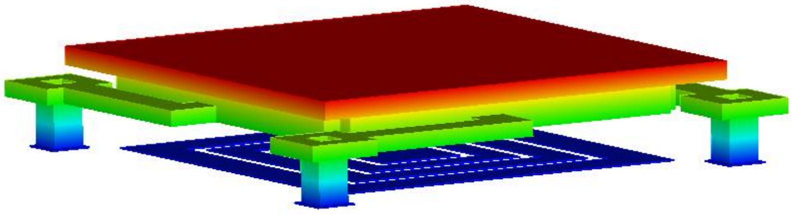

Figure 1. Illustration of a single element of the micro-machined spatial light modulator (µSLM).

3. BACKGROUND

As reported earlier by Cornelissen and et al(1) of Boston Micromachines Corp, the design of a micromirror structure was studied to achieve 0.78 µm stroke at an update rate of 44kHz. Further study has been done to improve the performances of the micromirrors. In the latest pixel structure design, a thickened actuator membrane has replaced a thin mirror post to reduce damping effect. This change results in improved piston motion uniformity and an increase in first out-of-plane natural frequency to 105KHz. In the new manufacturing process flow design, modifications have been made to address two issues in the previous fabrication process: 1) reflow of the photoresist when processing temperatures exceeded ~90ºC, and 2) excessive print-through from topography on underlying layers (i.e. actuator and anchors). Both of these modifications have improved the final mirror optical surface finish. In the new

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process, polyimide is used as sacrificial material replacing photoresist. The new sacrificial material allows metal deposition at high temperatures as well as a dry release process for the MEMS devices, and also it makes the print-through reduction possible.

4. FABRICATION PROCESS

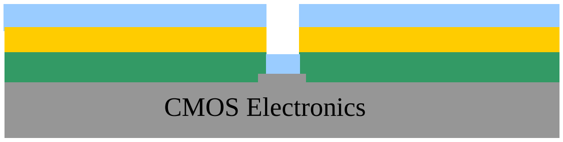
The microfabrication process has been developed to integrate a metal μSLM with the pre-fabricated CMOS electronics. The process consists of several steps: CMOS planarization, contact via etch, electrode and anchor fill, flexure, actuator thickener, mirror, and release. These steps are performed using standard semiconductor fabrication processes, including dielectric coating/polishing, photolithograhy, polyimide coating/curing, metal deposition/liftoff, dry/wet etch. All of the process steps are performed at low temperature to maintain the integrity of the CMOS device.

Foundry-delivered CMOS electronics chip have large surface topography (>590nm RMS) due to the underlying layers of polysilicon and metal. This CMOS is planarized by first depositing an extra overglass layer of thick(5µm)PECVD silicon nitride and then polishing the overglass to a finish of 15nmRMS using Chemical-Mechanical Polishing (CMP).

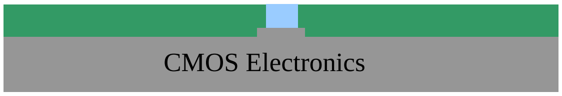
The contact via process is outlined in Figure 2. Vias are created first by patterning and etching through the planarization layer to an underlying electrode (step 1 and 2). Metal is deposited to make an electrical connection to the CMOS electronics and fill up the via hole (step 3). Then the residual metal and photoresist are removed (step 4).

1. Spin Photoresist and pattern electrode via

2. Etch Nitride to form via – stop on CMOS electrode



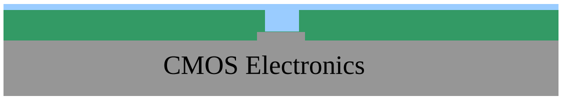
3. Deposit Aluminum



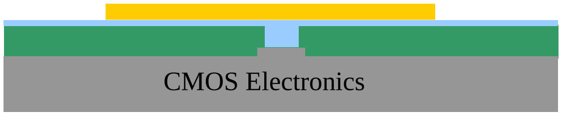
4. Lift-off residual Aluminum and photoresist

Figure 2. Contact via fabrication process

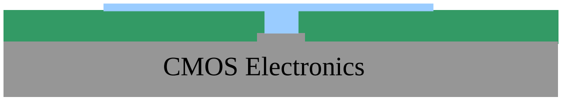
Following the via fill an array of segmented electrodes is fabricated such that all electrodes on each of the 22,500 pixels contact the via, electrically connecting the actuator electrode to the drive electronics. Figure 3 illustrates the manufacturing processes used to create these electrodes.



1) Deposit 100nm thick Aluminum 1 layer on planarized electronics chip



2) Spin on photoresist layer and pattern electrodes



3) Etch aluminum and remove photoresist to form electrodes

Figure 3. Illustration of Electrode fabrication process

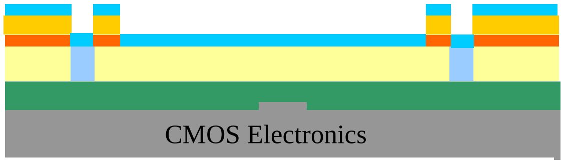
Actuator anchors are filled in a similar manner to that of contact vias. Instead of etching a silicon nitride layer, however, the 1st sacrificial layer of cured polyimide, is patterned, etched, and filled using the same process used for the vias. After filling the actuator anchors a thin layer of Polyimide 2556 is spun on and partially cured. This partial cure allows the polyimide to be etched using photoresist developer. A layer of photoresist is then spun on and lithographically patterned. As the resist is submerged in the developer, exposing the actuator pattern, the polyimide is also etched. Since the underlying polyimide layer is fully cured, the etch stops on this layer. Aluminum is then deposited to form the actuator flexures and the remaining metal and photoresist is subsequently removed using Acetone, leaving a planar surface with minimal surface topography after polyimide is cured (Figure 4).

The actuator thickener fabrication process will use the same processes used to manufacture the actuator anchors. This is illustrated in Figure 5 1-3. Polyimide is spun onto the die containing the first and second layers of the device (electrodes and actuators) and cured. Actuator thickeners are then patterned and etch at the center of the actuator membranes using oxygen plasma. The etched area is filled with sputtered metal after which a lift-off process removes the rest of the metal film as well as the photo resist. Following this process the die is coated with the 3rd aluminum film, which forms the mirror surface. The mirror segments are patterned following the metal deposition and etched using a wet aluminum etchant. After removal of the photoresist the sacrificial polyimide layers will be removed using Oxygen plasma in a barrel asher, isotropically etching the polyimide, leaving the free standing released MEMS mirror array on the CMOS die.

1. Complete Anchor etch and fill

2. Spin on and soft bake PI2556, 850nm thick polyimide, and 2µm thick photoresist,

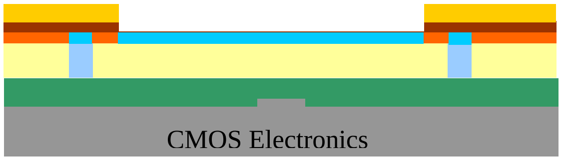
3. Pattern photo resist and etch polyimide



4. Deposit Actuator metal

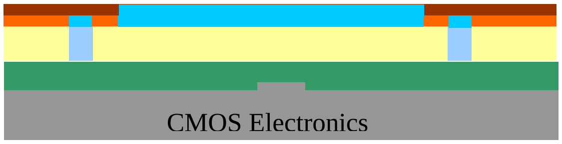
5. Remove remaining aluminum and photoresist using Lift-off

Figure 4. Actuator thickener process



1) Spin and cure 3rd polyimide film and photoresist. Pattern and etch actuator thickener.

2) Deposit 0.85µm of aluminum.



3) Remove metal and photoresist by lift-off

4) Deposit 1µm thick metal 3 layer and pattern mirror segments using photoresist.

5) Etch mirror segments and remove photoresist mask. Release device using Oxygen plasma

Figure 5. Illustration of mirror fabrication process & device release

5. RESULTS

To evaluate the success of the new manufacturing process in terms of improved optical quality, surface measurements were taken at many steps in the fabrication process using a Wyko 3-D surface interferometer. Figure 6 shows a comparison of the electrical contact vias etched in nitride without and with the new via fill process.

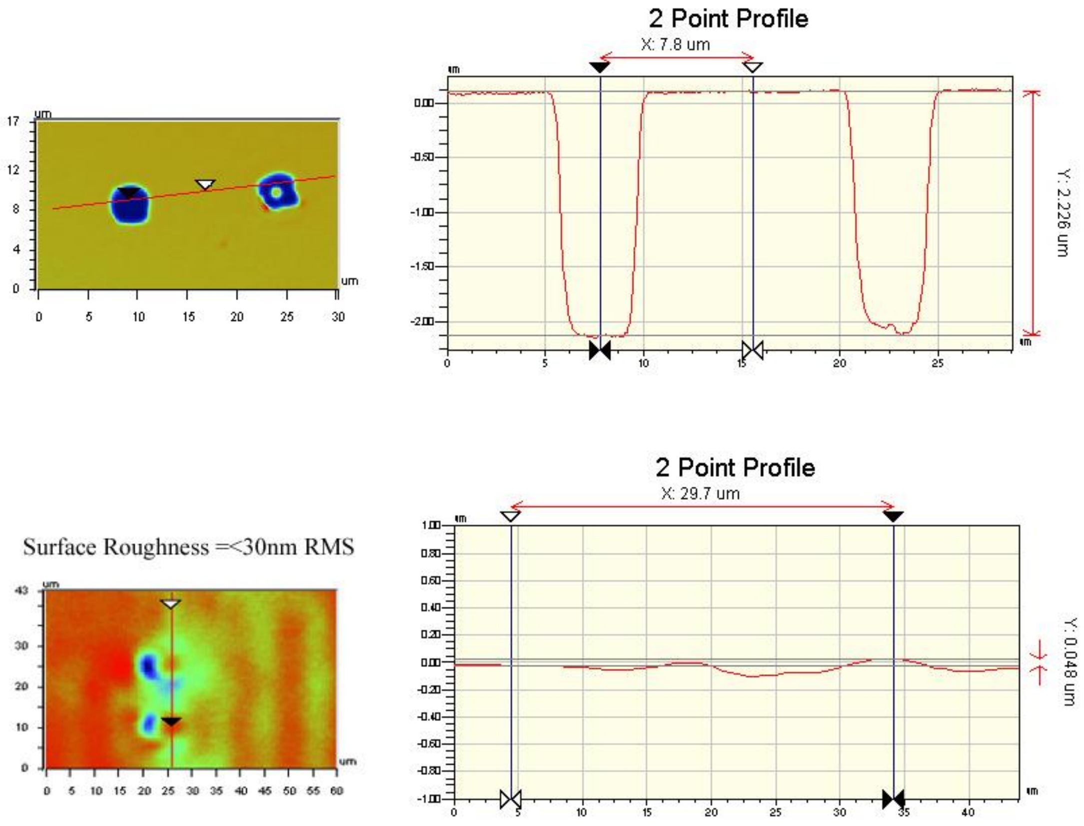


Figure 6. *Surface topography of Nitride surface. Top – Vias that are not filled. Bottom – Vias that were filled using new process*

Figure 7 shows the results of the anchor fill process. The measurement is of the second metal layer and shows a reduction in print through to ~90nm PV from more than 2 µm.

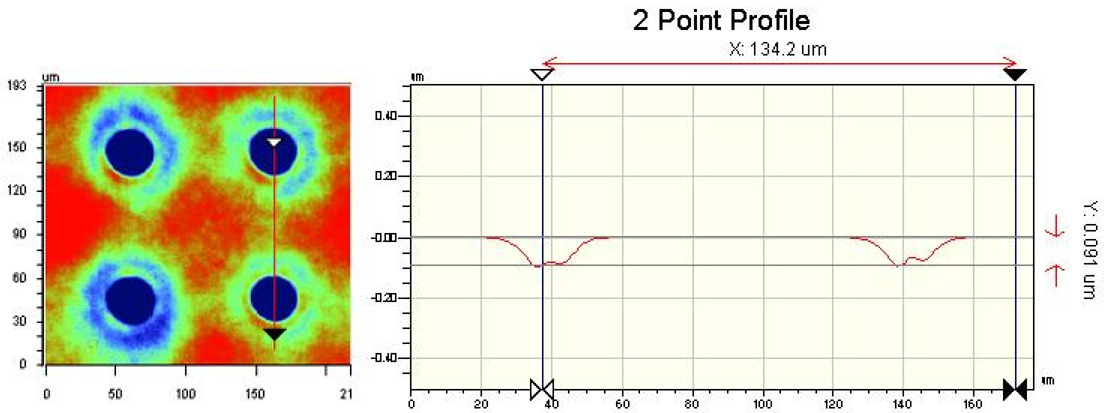


Figure 7. Surface topography of surface of a pixel after anchor fill process

The reduction in print through can also be seen in Figure 8, where the third metal layer is shown. The flexure manufacturing process reduces the print-through to 50 nm from 850 nm.

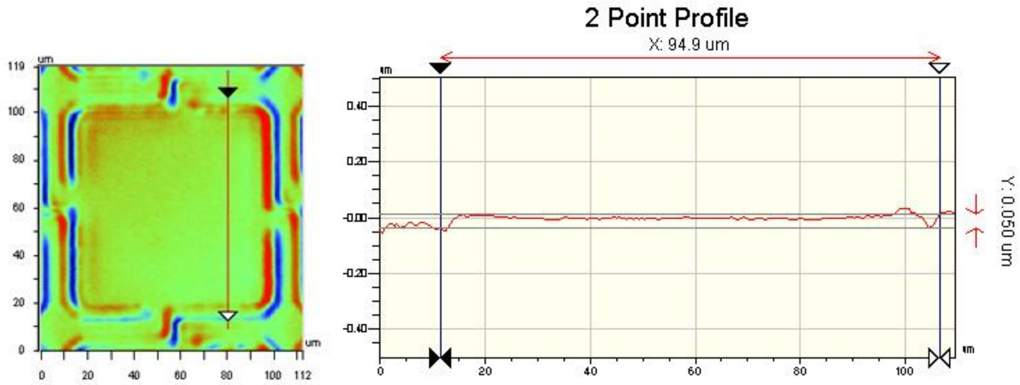


Figure 8. Surface topography of surface of a pixel after flexure process

As a result, these new fabrication processes leave for following process steps a smooth and planar surface onto which final metal layer can be deposited thereby minimizing the print-through onto the final mirror surface.

6. MEASUREMENTS

The electromechanical performance the integrated SLM was tested with a custom PCB connected to a computer to address the CMOS driver electronics. Figure 9 shows the setup for the measurements. Individual pixels could be addressed with the appropriate data inputs. Electromechanical testing was performed on 32x32 arrays of actuators integrated with CMOS electronics. The devices that were tested were integrated with non-planarized CMOS die. Since the CMOS planarization and via etch effort was still under development at the time, it was decided to start fabricating actuator arrays on the relatively rough overglass (Nitride) surface.

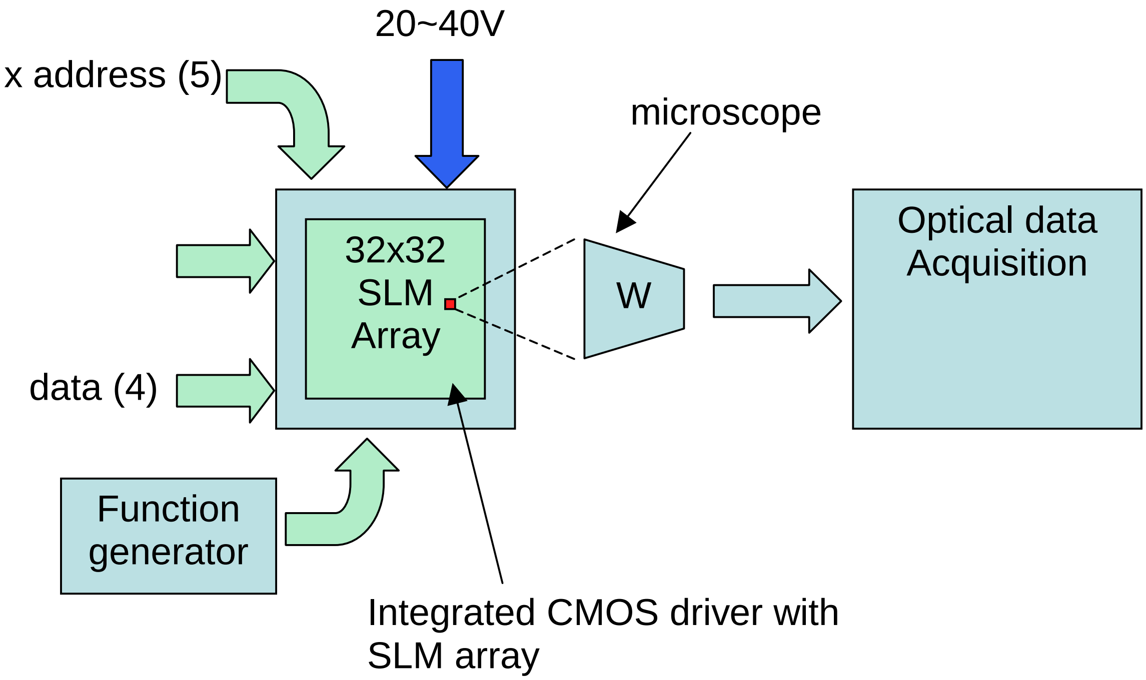
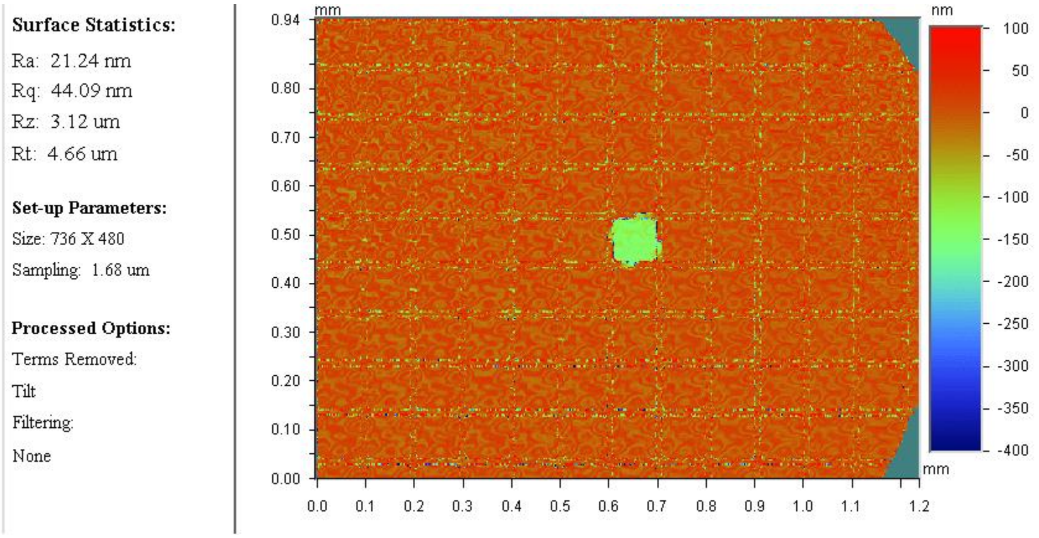


Figure 9. Schematic of integrated SLM test setup

Individual pixels were addressed as shown in Figure 10 and no cross talk or other influence on the neighboring pixels was measured. Using an electrode voltage of 30V, each of the four electrodes were individually address and the resulting deflection measure. This data is shown in Figure 11. Since the tested devices were integrated on a non-planarized CMOS passivation layer, the surface-normal gap between the electrodes and the actuator was non-uniform. For this reason only 30V was used and the total stroke was limited.



Surface Statistics:

Ra: 21.24 nm

Rq: 44.09 nm

Rz: 3.12 um

Rt: 4.66 um

Set-up Parameters:

Size: 736 X 480

Sampling: 1.68 um

Processed Options:

Terms Removed:

Tilt

Filtering:

None

Figure 10. Single pixel addressed with no influence on its neighboring actuators

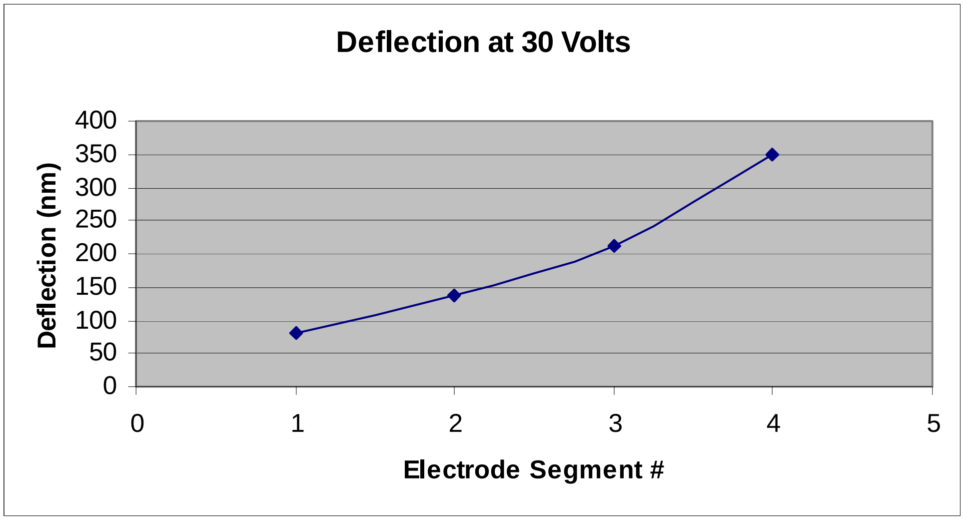


Figure 11. Actuator deflection vs electrode energized

7. FUTURE WORK

A new print-through reduction process has been developed, and individual pixel actuation has been demonstrated so far, the future effort will be combine the success in these two aspects to integrate a large array of SLM onto the planarized CMOS, meeting the design goals.

8. ACKNOWLEDGEMENTS

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9. REFERENCES

[1] Steven Cornelissen, Thomas Bifano, Paul Bierden, “MEMS spatial light modulators with integrated electronics”. Proc. SPIE Vol. 4561, p. 28-34, MOEMS and Miniaturized Systems II, M. Edward Motamedi; Rolf Goering; Eds