Large-scale metal MEMS mirror arrays with integrated electronics

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Abstract

Design, microfabrication, and integration of a micromachined spatial light modulator (μSLM) device are described. A large array of electrostatically actuated, piston-motion MEMS mirror segments make up the optical surface of the μSLM. Each mirror segment is capable of altering the phase of reflected light by up to one wavelength for infrared illumination (λ = 1.5 μm), with 4-bit resolution. The device is directly integrated with complementary metal-oxide semiconductor (CMOS) electronics, for control of spatial optical wavefront. Integration with electronics is achieved through direct fabrication of MEMS actuators and mirror structures on planarized foundry-type CMOS electronics. Technical approaches to two significant challenges associated with manufacturing the μSLM are discussed: integration of the MEMS array with the electronic driver array and production of optical-quality mirror elements using a metal-polymer surface micromachining process.

Introduction

Large arrays of micromachined piston-motion mirrors are required for laser communication and optical correlation applications. Such devices can be used to rapidly modify the spatial phase of a coherent wavefront. Spatial phase modulation has been possible for some years, primarily through the use of liquid crystal phase devices. MEMS-based spatial light modulators promise orders-of-magnitude higher speed, enabling the use of SLMs in applications such as pattern recognition and laser communication, which typically require faster response than is achievable using liquid crystal devices. To control large numbers of pixels in a MEMS SLM array it will be necessary that the pixels are addressed through direct integration, rather than off-chip addressing through wire bond connections. Such integration poses a system-level design challenge since silicon foundry MEMS processes are in general incompatible with prefabricated CMOS electronics (due to the high temperature processing required in MEMS fabrication). A MEMS fabrication alternative based on metal micromachining has proven successful in the past for production of large micromirror arrays, most notably for the Texas Instruments Digital Light Processor®. In the work described here, a process similar to that used for the TI-DLP is proposed, using foundry electronics chips as the MEMS substrate and employing low-temperature metal/polymer thin-film surface micromachining for MEMS device fabrication.

Design, Test, Integration, and Packaging of MEMS/MOEMS 2002, Bernard Courtois, Jean Michel Karam, Karen W. Markus, Bernd Michel, Tamal Mukherjee, James A. Walker, Editors, Proceedings of SPIE Vol. 4755 (2002) © 2002 SPIE · 0277-786X/02/$15.00

System Design and Process Flow Summary

The spatial light modulator (μSLM) under development consists of an array of 1024 piston motion MEMS mirror segments fabricated in aluminum over a 4 mm square aperture. Each pixel is capable of altering the phase of reflected light by up to one wavelength for visible light, controlled by an underlying digital CMOS driver that provides a 50 nm position resolution over 750 nm of stroke. Mirror elements are more than 90% reflective and are optically flat and smooth. The pixels are designed to have a step response time of 10μs. Mirror fill factor of 98% is achievable for square pixel sizes measuring 100 micrometers on a side. Because fabrication makes use of a low-temperature batch surface-micromachining process integrated with commercially available low-cost foundry electronics fabrication, the device is economical and scalable to megapixel array sizes. Figure 1 shows a schematic of nine mirror pixels in the μSLM.

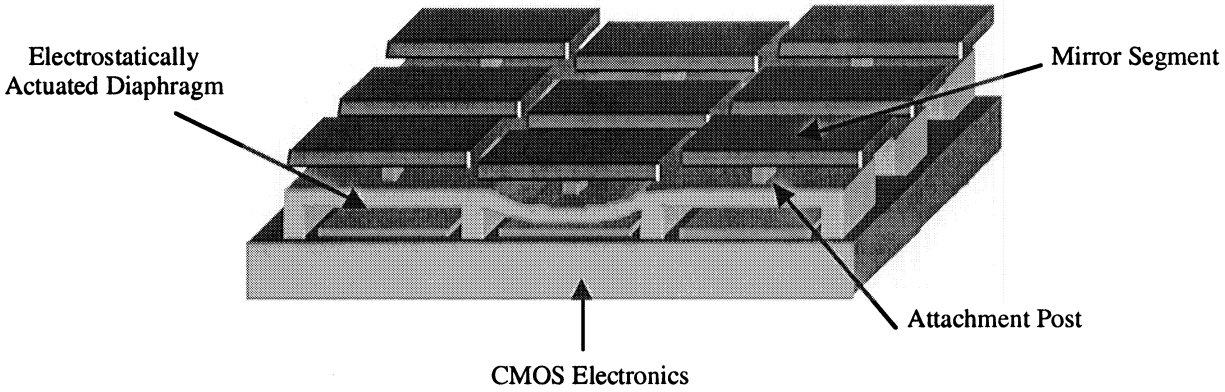


Figure 1. Cross-sectional schematic of three elements in a micro-machined spatial light modulator (μSLM).

The electronic driver array chip is fabricated through foundry CMOS processing at a commercial multi-user electronic chip fabrication foundry. The driver consists of a 4-bit digital random access memory (RAM) array, controlled at its periphery by a multiplexed address bus. Each bit in the RAM terminated in a metal pad at the surface of the chip, located beneath one of the μSLM electrode locations. CMOS device chips are shipped from the foundry with a protective overglass layer. This surface has significantly non-flat topography resulting from multi-layer CMOS fabrication process. Prior to fabricating the optical mirror array using a metal-polymer surface micromachining process, the surface of the CMOS electronics requires planarization. Planarization is achieved by sputter deposition of a thick glass layer, followed by polishing, patterning, and etching vias to the CMOS metal pads. The micromachining process steps are performed at low temperature to maintain the integrity of the CMOS device. Vias are created first by patterning and etching through the planarization layer to an underlying electrode in the CMOS driver array. Metal is patterned in a lift-off process to make electrical connection to the CMOS and to form electrodes. Metal deposition is achieved using sputtering. The actuation electrode is divided into concentric electrodes, which are connected electrically to the underlying CMOS driver. Each ring has successively larger area, in a geometric

sequence. After electrode deposition, patterned photoresist sacrificial layers are alternated with patterned metal structural layers to form an array of fixed-fixed beam parallel plate actuators beneath a corresponding array of mirror segments. Ultimately, the sacrificial layers are etched away, leaving a self-assembled, integrated optoelectromechanical device.

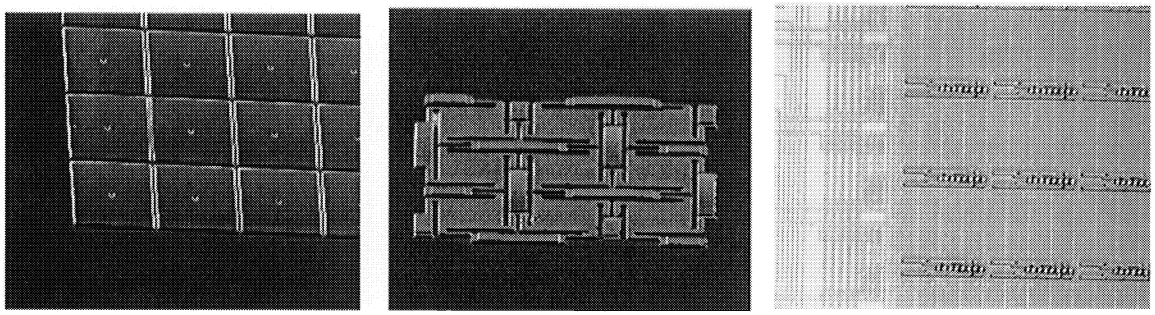


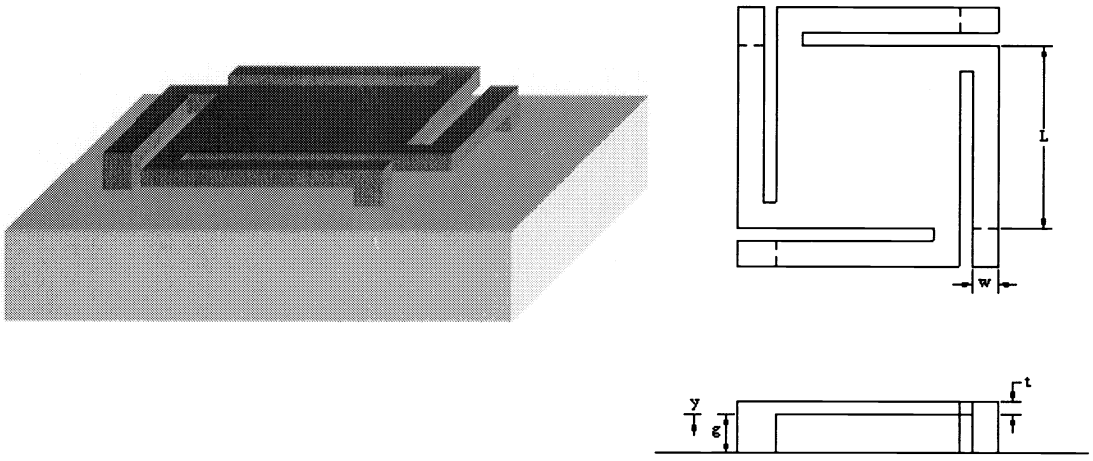
Figure 2: Test structures fabricated for the μSLM. Left: 32 x 32 element micromirror array. Center: 3 x 3 actuator array. Right: CMOS driver array.

Model of μSLM pixel

A mathematical model of the proposed actuator was developed to assist in design studies and to predict electromechanical behavior. Figure 3 shows the configuration of the actuator design in which a square membrane is supported by four flexures running parallel to the electrostatic diaphragm of the actuator. In the proposed design, each individual mirror pixel is actuated electrostatically using electrodes located beneath the square membrane. The mirrors are attached to the actuator by a post attached to the center of the membrane (not shown in figure). The actuator deflection can be determined through a force balance equation between the mechanical restoring force, F_m, and the electrostatic force, F_e establishing an electromechanical equilibrium for the actuator. The mechanical restoring force is applied to the movable actuator plate through four anchored flexure arms, modeled as fixed-guided cantilever beams; the actuator plate is assumed to be rigid.

$$F_e = F_m \qquad F_e = \frac{\varepsilon A V^2}{2(g-y)^2} \qquad F_m = \frac{4Ewt^3}{L^3} y$$

Where ε is the dielectric constant of the actuator gap, V is the voltage applied to the actuator, L is the length of the flexure arm, g is the gap between the actuator diaphragm and the substrate, y is the surface-normal deflection of the actuator plate, E is the modulus of elasticity of the actuator material, w is the width of the flexure arm, and t is the thickness of the flexure arm.



Parameter	Value
Driving voltage, V	40 V
Stroke	0.78μm
Minimum gap, g	2.5μm
Actuation area, A	80μm x 80μm
Natural frequency	100 kHz

Figure 3. Schematic and design specifications of μSLM actuator

Integration of MEMS and Electronics

The vertical integration of the mechanical structure with CMOS electronics requires the appropriate mechanical interface and electrical interface. Before MEMS fabrication, the overglass protective layer of a CMOS chip is first augmented (if necessary) to thicken this rough layer, which has unacceptable topography due to the CMOS electronic devices underneath. The composite SiO_2 layer is then lapped and polished to planarize it in preparation for MEMS processing.

Figure 4 (top) shows the surface of the CMOS chip with aluminum pattern and vias as delivered from the foundry. This pattern is repeated at a pitch of 81.6 μm in the horizontal direction and 85.2 μm in the vertical direction. These dimensions represent the mirror size. The CMOS chip has a 1.6 μm thick passivation layer consisting of Si_3N_4 and SiO_2 layers. Figure 4 (bottom) is a profile of the passivation surface showing the depth of the etched via.

The topography of the CMOS surface from a commercial foundry is not suitable for a MEMS structure with flat metal electrodes and mirrors. It is therefore planarized using low temperature deposition and polishing processes. The planar surface must be parallel to the top of the aluminum pattern within 1 μm over a 3 mm by 3 mm area. The

requirements for root-mean-square figure accuracy and roughness on each pixel area are λ/100 (15 nm) and 1 nm, respectively. Following planarization, vias are etched through the new deposition layer and then filled with metal to provide electrical connection. The etched via-cuts must align to square aluminum pads 3 μm on a side that have as little as 3 μm space between them.

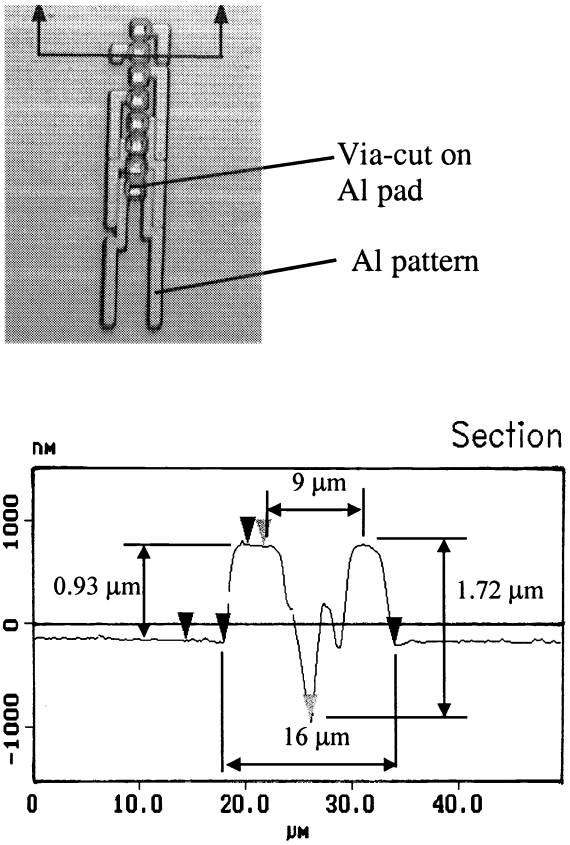


Figure 4: Microphotograph and cross sectional profile measured with an atomic force microscope for a CMOS electronics test chip.

Figure 5 shows the process flow for obtaining a planarized CMOS with via cuts. For the development of this process, we prepared a number of test structures whose purpose is to replicate the relevant characteristics of the CMOS chips. Figure 5 also shows the steps for making the test structures.

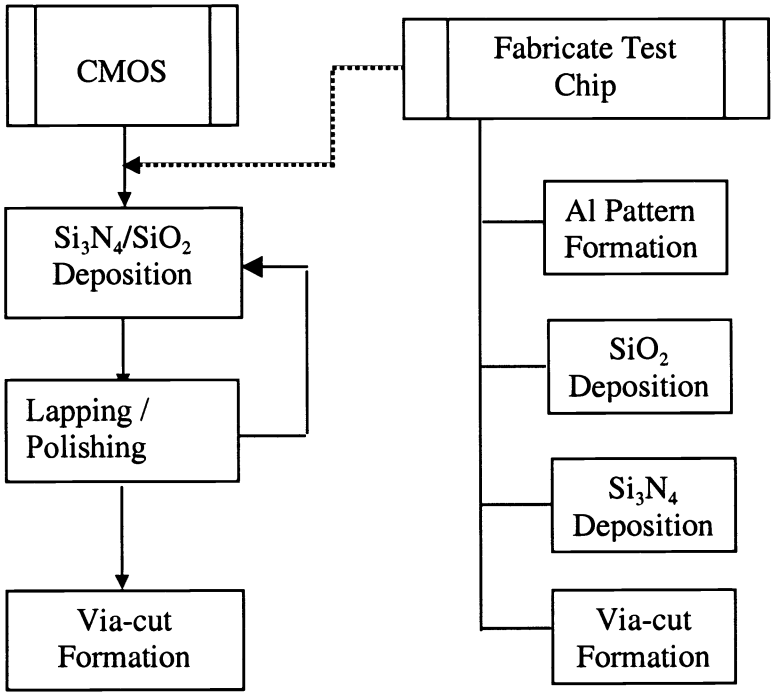


Figure 5: Process flow for the vertical integration of the metal MEMS with CMOS

Figure 6(top) shows one of the planarization test chips. Each pixel area has a pattern of three aluminum bars, each nominally 3 μm wide and 0.8 μm tall, formed by sputtering. A 1.6 μm thick passivation layer was formed by sputtering silicon dioxide and silicon nitride. Figure 6(bottom) shows a profile of the test surface before etching vias.

Preliminary planarization efforts on a test chip yielded parallelism of 80 nm over a 3 mm by 3 mm area, average figure accuracy of 37 nm (P-V for 200μm line scans), and average Ra roughness of 2.1 nm (for 100 μm line scans). As a comparison, for SiO_2 deposited on a flat silicon wafer, the flatness and roughness were 44 nm and 3.0 nm, respectively.

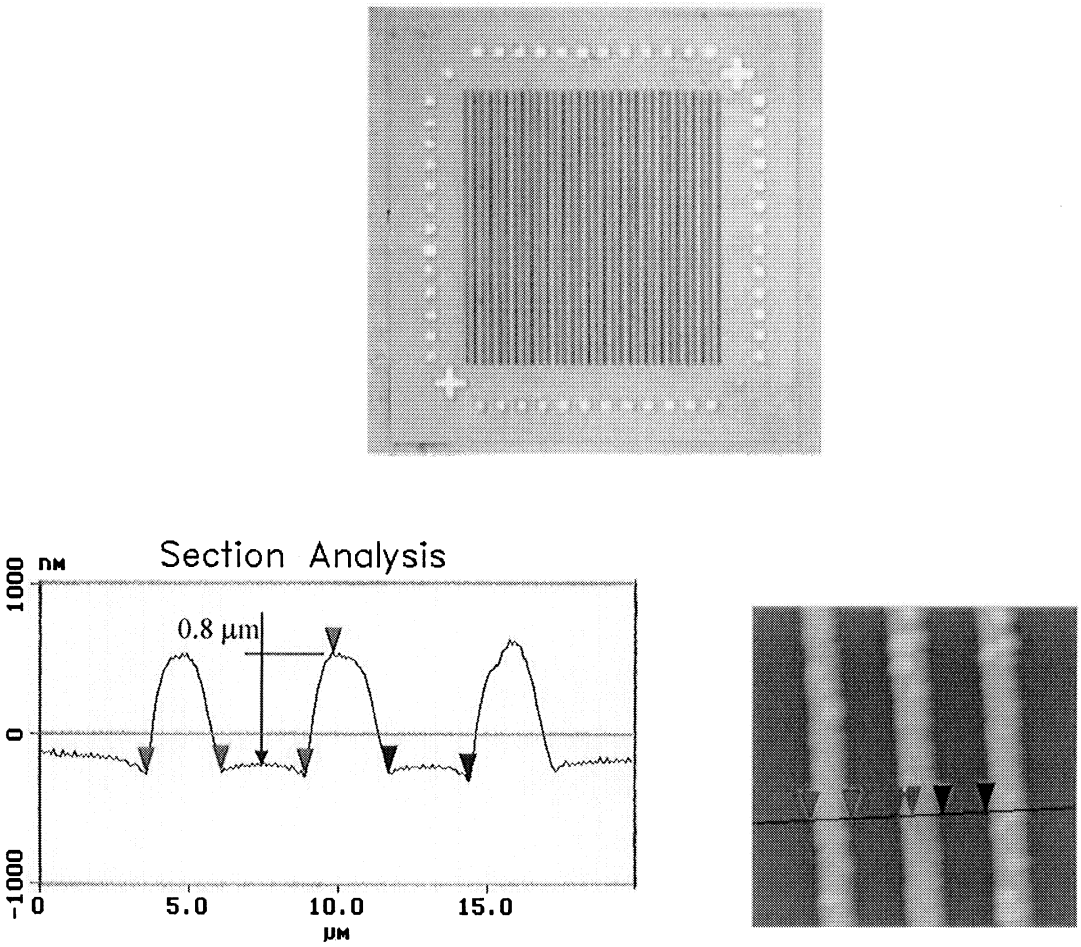


Figure 6. Planarization test chips for developing MEMS interface processes. Top: Micrograph of test chip (4 x 4 mm). Bottom: AFM profile of the passivation layer of the test chip (no via-cut)

MEMS Fabrication Details

The MEMS fabrication process is outlined in Figures 7a & b. Via formation and electrode fabrication steps are outlined in figure 7a. The vias are created by patterning and etching through the planarization layer to an underlying electrode. A layer of resist is than spun on and patterned, followed by a metal deposition to form the electrodes using lift-off. A sacrificial layer of photoresist is spun on, the thickness of which determines the actuator gap, as shown in figure 7b. The actuator anchors are patterned and a third metal layer, 1.0 µm thick, is deposited. The metal 2 layer is than patterned and etched to form the actuator. Another sacrificial layer of resist is spun on and patterned to form the mirror posts after a second metal etching process. Finally, sacrificial resist layers are removed leaving an assembled MEMS device.

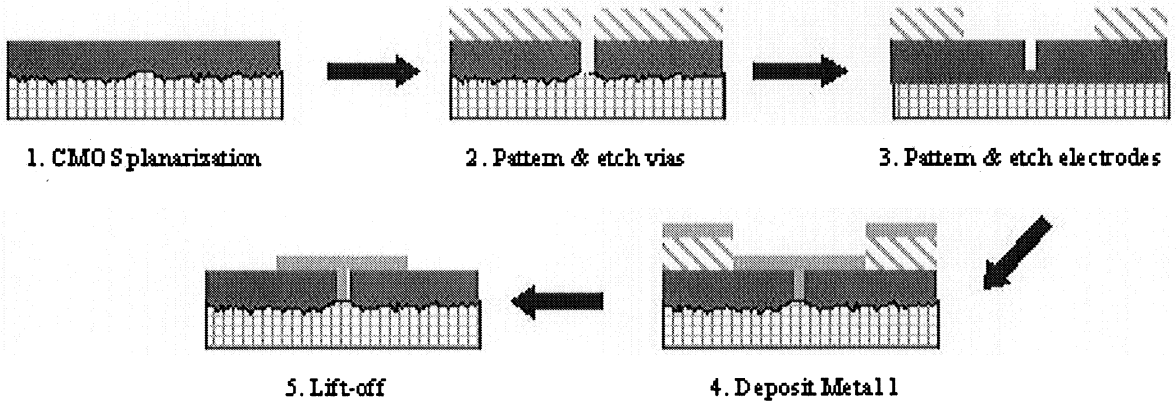


Figure 7a. μSLM via and electrode fabrication process

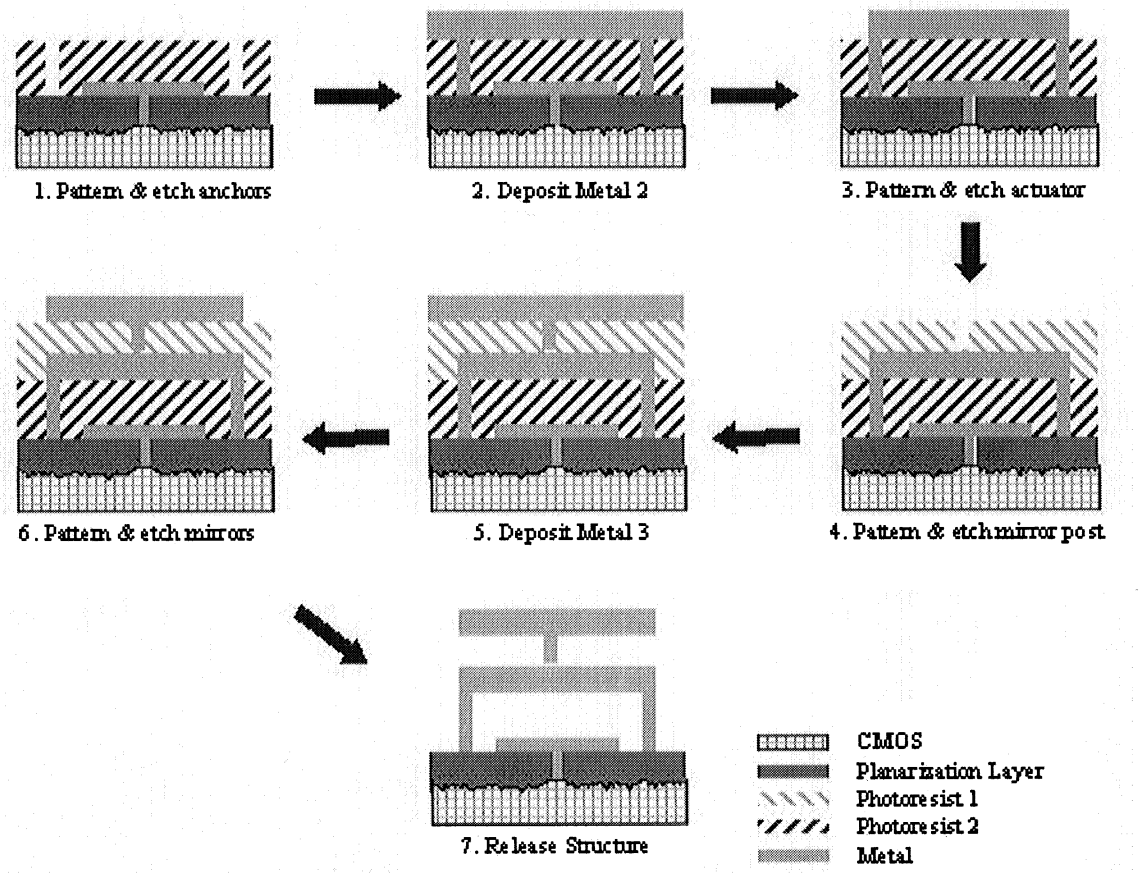


Figure 7b. μSLM actuator and mirror fabrication

Proof-of-concept μSLM actuator

To develop a proof-of-concept μSLM actuator, aluminum was deposited on a patterned photoresist film atop a glass substrate. Lithographic patterning of the deposited metal film was achieved by wet-etching of the metal through a second photoresist mask. After metal patterning, the devices were released by dissolving all photoresist in an acetone bath. Critical point drying was used to prevent stiction in the released device. Using this process, a series of actuators and mirrors were fabricated individually and in small arrays. A surface contour interferometric map of one of the actuators is shown in Figure 8. The device consists of a 1.3μm thick aluminum membrane supported by four springs above three concentric electrodes (not shown). The aluminum film was measured to be optically flat to within 30 nm RMS over its active surface.

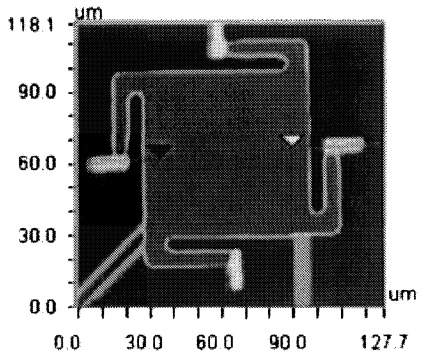


Figure 8: Interferometric microscope measurement of proof-of-concept metal actuator

The electromechanical performance of a microactuator was characterized. Stroke and resolution were measured using an interferometric microscope during electrostatic actuation. Figure 9 shows the measured and predicted displacement of the actuator for constant supply voltage of ~40 V applied in a binary sequence to three electrodes E1, E2, and E3. It is believed that mask definition and alignment errors are responsible for the differences observed between measured and predicted response.

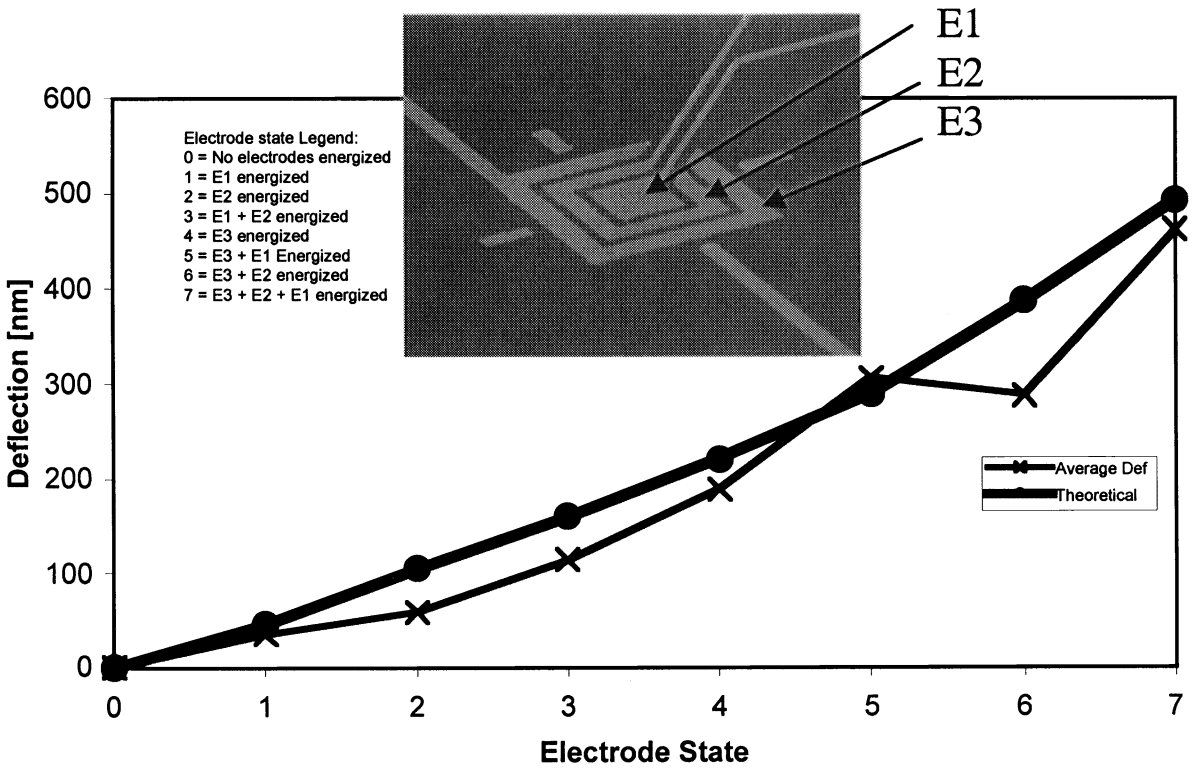


Figure 9: Measured and predicted response of 3-bit electrostatic proof-of-concept metal μSLM actuator.

Conclusion

A multifaceted program directed toward integration of large-scale MEMS micromirror arrays and commercially-available CMOS electronics has been described. Challenges associated with actuator design and fabrication, low temperature (CMOS compatible) MEMS fabrication, and CMOS chip planarization have been addressed. These manufacturing processes will be combined to produce a micromachined spatial light modulator.